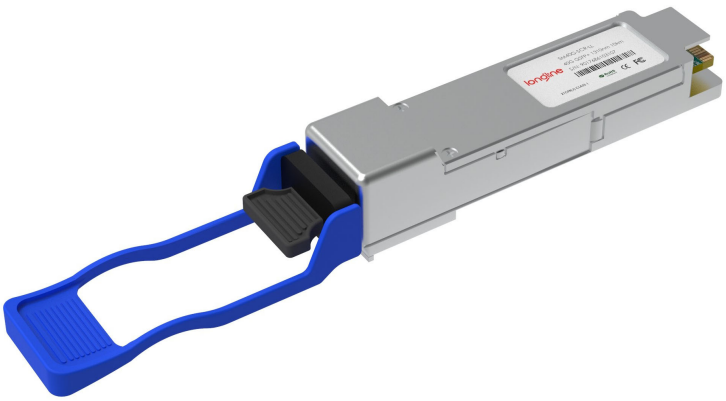
40GBASE-CSR4 QSFP+ 850nm 400m MTP/MPO Transceiver for MMF

SM40G-SCR-LL



Application

- 40GBASE-SR4 40G Ethernet
- Breakout to 10GBASE-SR Ethernet
- Proprietary interconnections

Features

- Four-channel full-duplex transceiver module
- Hot Pluggable QSFP+ form factor
- Maximum link length of 300m on OM3 Multimode Fiber (MMF) and 400m on OM4 MMF
- Multirate capability: 1.06Gb/s to 10.5Gb/s per channel
- Unretimed XLPPI electrical interface
- Max power dissipation <1.2W
- Reliable VCSEL array technology
- RoHS-6 Compliant
- Built-in digital diagnostic functions, including optical power monitoring
- Commercial operating case temperature range: 0°C to 70°C
- Single 1x12 MPO receptacle

Description

QSFP+ transceiver modules are designed for use in 40 Gigabit per second links over multimode fiber, including breakout to four 10 Gigabit per second links. They are compliant with the QSFP+ MSA and IEEE 802.3ba 40GBASE-SR4 and compatible with IEEE 802.3ae 10GBASE-SR. The optical transceiver is compliant per the RoHS Directive 2011/65/EU.

Product Specifications

I.General Specifications

Parameter	Value	Unit	Notes
Module Form Factor	QSFP+		
Number of Lanes	4 Tx and 4 Rx		
Maximum Aggregate Data Rate	42.0	Gb/s	
Maximum Data Rate per Lane	10.5	Gb/s	Higher bit rates may be supported. Please contact Longline.
Protocols Supported	Typical applications include 40G Ethernet, Infiniband Fibre Channel, SATA/SAS3		
Electrical Interface and Pin-out	38-pin edge connector		Pin-out as defined by the QSFP+ MSA
Maximum Power Consumption	1.2	Watts	Varies with output voltage swing and pre-emphasis settings
Management Interface	Serial, I2C-based, 400 kHz maximum frequency		As defined by the QSFP+ MSA

Data Rate Specifications	Symbol	Min	Typ.	Max	Unit	Ref.
Bit Rate per Lane	BR	1062		10500	Mb/sec	1
Bit Error Ratio	BER			10-12		2
Link distance on OM3 MMF	d			300	meters	3
Link distance on OM4 MMF	d			400	meters	3

Notes:

1.Compliant with 40G and 10G Ethernet. Compatible with 1 Gigabit Ethernet and 1/2/4/8/10G Fibre Channel.

2.Tested with a PRBS 231-1 test pattern.

3.Per 40GBASE-CSR4 and 10GBASE-SR IEEE 802.3ba.

II. Absolute Maximum Ratings

Parameter	Symbol	Min	Typ.	Max	Unit	Ref.
Maximum Supply Voltage	Vcc1, VccTx, VccRx	-0.5		3.6	V	
Storage Temperature	T_S	-40		85	° C	
Case Operating Temperature	Top	0		70	° C	
Relative Humidity	RH	0		85	%	1
Damage Threshold, per Lane	DT	3.4			dBm	

Note:

Non-condensing

III. Electrical Characteristics (TOP= 0 to 70 ° C, VCC = 3.15 to 3.45 Volts)

Parameter	Symbol	Min	Typ.	Max	Unit	Ref.
Supply Voltage	Vcc1, VccTx, VccRx	3.15		3.45	V	
Supply Current	Icc			350	mA	
Transmit turn-on time				2000	ms	1
Transmitter (per Lane)						
Single ended input voltage tolerance	VinT	-0.3		4.0	V	
Differential data input swing	Vin,pp	180		1200	mVpp	2
Differential input threshold			50		mV	
AC common mode input voltage tolerance (RMS)		15			mV	
Differential input return loss		Per IEEE P802.3ba,Section 86A.4.1.1			dB	3
J2 Jitter Tolerance	Jt2	0.17			UI	

Transmitter (per Lane)

J9 Jitter Tolerance	Jt9	0.29			UI	
Data Dependent Pulse Width Shrinkage	DDPWS	0.07			UI	
Eye mask colordinates {X1, X2 ,Y1, Y2}		0.11, 0.31 95, 350			UI mV	4

Receiver(per Lane)

Single-ended output voltage		-0.3		4.0	V	
Differential data output swing	Vout,pp	0		800	mVpp	5.6
AC common mode output voltage (RMS)				7.5	mV	
Termination mismatch at 1 MHx				5	%	
Differential output return loss		Per IEEE P802.3ba,Section 86A.4.2.1			dB	3
Common mode output return loss		Per IEEE P802.3ba,Section 86A.4.2.2			dB	3
Output transition time, 20% to 80%		28				
J2 Jitter output	Jo2			0.42	UI	
J9 Jitter output	Jo9			0.65	UI	
Eye mask coordinates #1 {X1, X2, Y1, Y2}		0.29, 0.51 50, 425			UI mV	4
Power Supply Ripple Tolerance	PSR	50			mVpp	

Notes:

1.From power-on and end of any fault conditions.

2.After internal AC coupling. Self-biasing 100Ω differential input.

3.10 MHz to 11.1 GHz range

4.Hit ratio = 5 x 10E-5.

5. AC coupled with 100Ω differential output impedance.

6.Settable in 4 discrete steps via the I2C interface.

IV. Optical Characteristics (TOP = 0 to 70 ℃, VCC = 3.1 to 3.47 Volts)

Parameter	Symbol	Min	Typ.	Max	Unit	Ref.
Transmitter (per Lane)						
Signaling Speed per Lane		1.00	10.3125	10.5	GBd	
Center wavelength		840		860	nm	
RMS Spectral Width	SW			0.40	nm	
Average Launch Power per Lane	TXP_x	-7.5		0	dBm	1
Transmit OMA per Lane	TxOMA			3.0	dBm	2
Difference in Power between any two lanes (OMA)	TP_x			4.0	dB	
Peak Power per Lane	PP_x			4.0	dBm	
Launch Power (OMA) minus TDP per Lane	P-TDP	-6.5			dBm	
TDP per Lane	TDP_{SR4}			3.5	dBm	3
Sidemode Suppression ratio	TDP_{SR4}			3.9		4
Optical Extinction Ratio	ER	3.0			dB	
Optical Return Loss Tolerance	ORL			12	dB	
Encircled Flux	FLX		> 86% at 19 um < 30% at 4.5 um		dBm	
Average launch power of OFF transmitter, per lane				-30	dBm	
Relative Intensity Noise	RIN			-128	dB/Hz	
Transmitter eye mask definition {X1, X2, X3, Y1, Y2, Y3}		{0.23, 0.34, 0.43, 0.27, 0.35, 0.4}				

Parameter	Symbol	Min	Typ.	Max	Unit	Ref.
Receiver (per Lane)						
Signaling Speed per Lane		1.00	10.3125	10.5	GBd	
Center wavelength		840		860	nm	
Damage Threshold	DT	3.4			dBm	
Average Receive Power per Lane	RXPx	-9.9		2.4	dbm	
Receive Power (OMA) per Lane	RxOMA			3.0	dBm	
Unstressed Receiver Sensitivity (OMA) per Lane(OMA) per Lane	URS	-11.1			dBm	
Stressed Receiver Sensitivity (OMA) per Lane	SRS	-7.5			dBm	
Peak Power, per lane	PPx			4	dBm	
Receiver Reflectance	Rfl			-12	db	
Vertical eye closure penalty, per lane				3.5	db	
Stressed eye J2 jitter, per Lane				0.3	UI	
Stressed eye J9 jitter, per Lane				0.47	UI	
OMA of each aggressor lane				-0.4	dBm	
Rx jitter tolerance: Jitter frequency and p-p amplitude		(75, 5)			kHz, UI	
		(375,1)			kHz, UI	
LOS De-Assert	LOSD			-12	dBm	
LOS Assert	LOSA	30			dBm	
LOS Hysteresis		0.5			dBm	

Notes:

1. The maximum launch power of 0 dBm is well within the guardband of receiver overload specifications for commercially available 10GBASE-SR SFP+transceivers.
2. Even if TDP is <0.9dB, the OMA min must exceed this value.
3. This TDP is up to 100m on OM3 and 150m on OM4.
4. This TDP is up to 300m on OM3 and 400m on OM4.

V. Pin Description

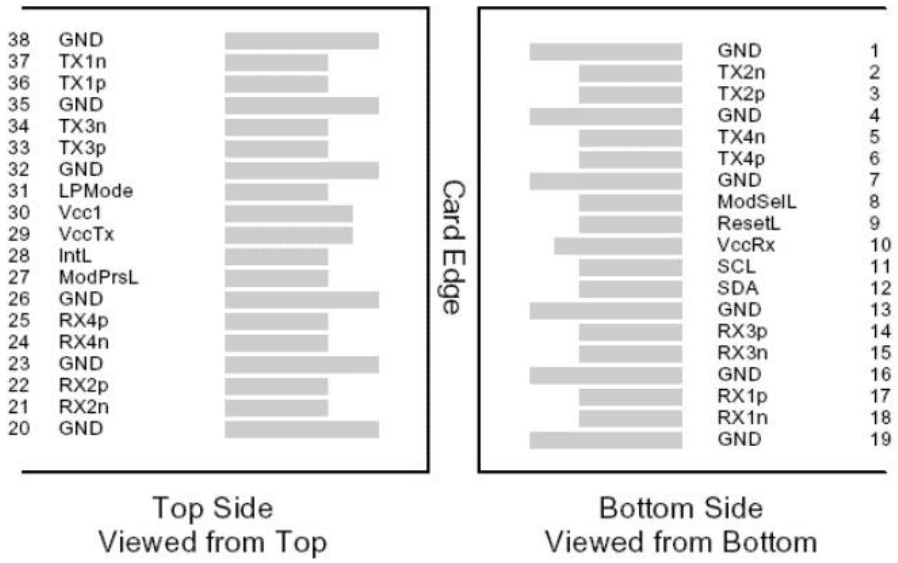


Figure 1 – QSFP+ MSA-compliant 38-pin connector

Pin	Symbol	Name/Description	Notes
1	GND	Ground	1
2	Tx2n	Transmitter Inverted Data Input	
3	Tx2p	Transmitter Non-Inverted Data Input	
4	GND	Ground	1
5	Tx4n	Transmitter Inverted Data Input	
6	Tx4p	Transmitter Non-Inverted Data Input	
7	GND	Ground	1
8	ModSelL	Module Select	
9	ResetL	Module Reset	
10	Vcc Rx	+3.3 V Power supply receiver	
11	SCL	2-wire serial interface clock	
12	SDA	2-wire serial interface data	
13	GND	Ground	1
14	Rx3p	Receiver Non-Inverted Data Output	
15	Rx3n	Receiver Inverted Data Output	

16	GND	Ground	1
17	Rx1p	Receiver Non-Inverted Data Output	
18	Rx1n	Receiver Inverted Data Output	
19	GND	Ground	1
20	GND	Ground	1
21	Rx2n	Receiver Inverted Data Output	21
22	Rx2p	Receiver Non-Inverted Data Output	
23	GND	Ground	1
24	Rx4n	Receiver Inverted Data Output	
25	Rx4p	Receiver Non-Inverted Data Output	
26	GND	Ground	1
27	ModPrsL	Module Present	
28	IntL	Interrupt	
29	Vcc Tx	+3.3 V Power supply transmitter	
30	Vcc1	+3.3 V Power Supply	
31	LPMode	Low Power Mode	
32	GND	Ground	1
33	Tx3p	Transmitter Non-Inverted Data Input	
34	Tx3n	Transmitter Inverted Data Input	
35	GND	Ground	1
36	Tx1p	Transmitter Non-Inverted Data Input	
37	Tx1n	Transmitter Inverted Data Input	
38	GND	Ground	1

Notes:

Circuit ground is internally isolated from chassis ground.

VI. Mechanical Specifications

The mechanical specifications are compliant to the QSFP+ MSA transceiver module specifications.