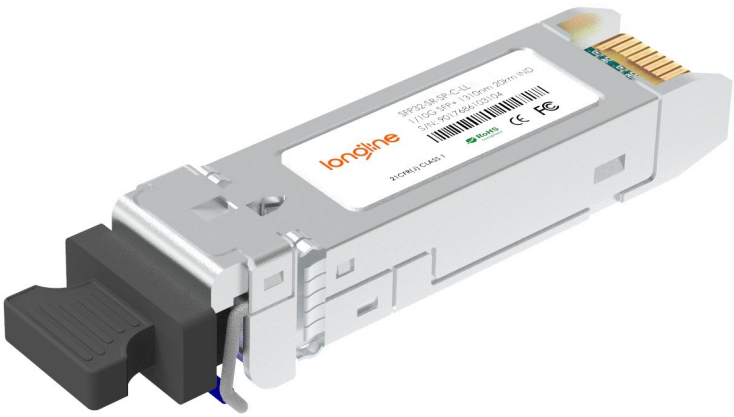
32GBASE-SR SFP28 850nm 100m DOM Transceiver

SFP32-SR-SP-C-LL



Application

- Tri-Rate 8G/16G/32G Fibre Channel

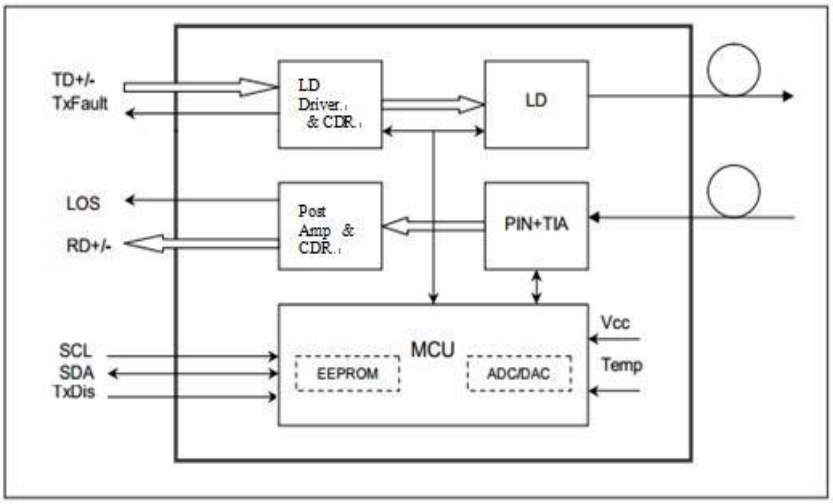
Features

- Up to 28.05Gb/s bi-directional data links
- Hot-Pluggable SFP28 form factor
- Built-in digital diagnostic functions
- 850nm VCSEL laser and PIN photo-detector
- Duplex LC receptacle
- Single 3.3V power supply
- Power dissipation < 1W
- RoHS-6 compliant
- Commercial case temperature range: 0° C to 70° C
- Internal CDR on both Transmitter and Receiver channel

Description

The SFP28-32G-SW is a single-channel, pluggable, fiber-optic for use in 8G/16G/32G Fibre Channel links up to 28.05Gb/s data rate over multimode fiber. They are compliant with FC-PI- 6a, SFF-8472 Rev 12.2c, and compatible with SFF-8432b and applicable portions of SFF-8431 Rev. 4.1d. The transceiver is RoHS compliant and per Directive 2011/65/EU.

Block Diagram



I. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Note
Supply Voltage	Vcc	0	3.6	V	
Storage Temperature	Ts	-40	+85	° C	
Operating Humidity	-	5	85	%	

II. General Specifications

Parameter	Symbol	Min	Typical	Max	Unit	Note
Commercial Temperature	Tc	0		+70	° C	
Power Supply Voltage	Vcc	3.13	3.3	3.47	V	
Power Supply Current	Icc			300	mA	
Fiber Length on 50/125µm high-bandwidth(OM3) MMF				150 100 70	m	1 2 3
Fiber Length on 50/125µm high-bandwidth(OM4) MMF				190 125 100	m	1 2 3

Notes:

1. At 8.5 Gb/s Fibre Channel data rate.
2. At 14.025 Gb/s Fibre Channel data rate.
3. At 28.05Gb/s Fibre Channel data rate..

III. Optical and Electrical Characteristics

Parameter		Symbol	Min	Typical	Max	Unit	Note
Transmitter							
Data Rate		BR		8.5 14.025 28.05		Gbps	
Centre Wavelength		λc	840	850	860	nm	
Spectral Width (RMS)		σ			0.6	nm	
Average Output Power **8.5** **14.025** **28.05**		P_{avg}	-8.2 -7.8 -6.7		2	dBm	
Optical Power OMA **8.5** **14.025** **28.05**		P_{OMA}	-5.2 -4.8 -3.2			dBm	
Extinction Ration		ER	2			dB	
Differential Data Input Swing **28.05Gb/s** **14.025Gb/s & 8.5Gb/s**		$V_{IN,PP}$	50 180		900 700	mV	
Input Differential Impedance		Z_{IN}	90	100	110	Ω	
TX Disable	**Disable**		2.0		Vcc	V	
	Enable		0		0.8	V	
TX Fault	**Fault**		2.0		Vcc	V	
	Normal		0		0.8	V	
Receiver							

Data Rate	BR		8.5 14.025 28.05		Gbps	1
Centre Wavelength	λc	840	850	860	nm	
Unstressed Receiver Sensitivity (OMA) 28.05Gb/s 14.025Gb/s 8.5Gb/s	RXsens			-10.2 -10.5 -11.2	dBm	
Average Receiver Power	Rx_{MAX}			2	dBm	
Bit Error Rate	BER			E-12 E-6		2 3
LOS De-Assert	LOS_D			-13	dBm	
LOS Assert	LOS_A	-30			dBm	
LOS Hysteresis		0.5			dB	
Differential Data Output Swing	Vout.pp	300		850	mV	
LOS	High	2.0		Vcc	V	
	Low	0		0.8	V	

Notes:

1. 8.5Gb.s Prbs7 for 8GFC, 14.025Gb/s Prbs31 for 16GFC, 28.05Gb/s Prbs31 for 32GFC;
2. For 32GFC with FEC, receiver sensitivity is defined at 10-6 BER level, not 10-12 BER level.

IV. Timing Requirement

Parameter	*Symbol*	*Min.*	*Max.*	*Unit*	*Conditions*
Tx_Disable assert time	t_off		100	µs	Rising edge of Tx_Disable to fall of output signal below 10% of nominal
Tx_Disable negate time	t_on		2	ms	Falling edge of Tx_Disable to rise of output signal above 90% of nominal. This only applies in normal operation, not during start up or fault recovery.
Time to initialize 2-wire interface	t_2w_start_up		300	ms	From power on or hot plug after the supply meeting Table 8.
Time to initialize	t_start_up		300	ms	From power supplies meeting Table 8 or hot plug or Tx disable negated during power up, or Tx_Fault recovery, until non-cooled power level I part (or non-cooled power level II part already enabled at power level II for Tx_Fault recovery) is fully operational.
Time to initialize cooled module and time to power up a cooled module to Power Level II	t_start_up_cooled		90	s	From power supplies meeting Table 8 or hot plug, or Tx disable negated during power up or Tx_Fault recovery, until cooled power level I part (or cooled power level II part during fault recovery) is fully operational. Also, from stop bit low-to-high SDA transition enabling Power Level II until cooled module is fully operational
Time to Power Up to Level II	t_power_level2		300	ms	From stop bit low-to-high SDA transition enabling power level II until non-cooled module is fully operational
Time to Power Down from Level II	t_power_down		300	ms	From stop bit low-to-high SDA transition disabling power level II until module is within power level I requirements
Tx_Fault assert	Tx_Fault_on		1	ms	From occurrence of fault to assertion of Tx_Fault
Tx_Fault assert for cooled module	Tx_Fault_on_cooled		50	ms	From occurrence of fault to assertion of Tx_Fault
Tx_Fault Reset	t_reset	10		µs	Time Tx_Disable must be held high to reset Tx_Fault
RS0, RS1 rate select timing for FC	t_RS0_FC, t_RS1_FC		500	µs	From assertion till stable output
RS0, RS1 rate select timing non FC	t_RS0, t_RS1		24	ms	From assertion till stable output
Rx_LOS assert delay	t_los_on		100	µs	From occurrence of loss of signal to assertion of Rx_LOS
Rx_LOS negate delay	t_los_off		100	µs	From occurrence of presence of signal to negation of Rx_LOS

V. Digital Diagnostic Specification

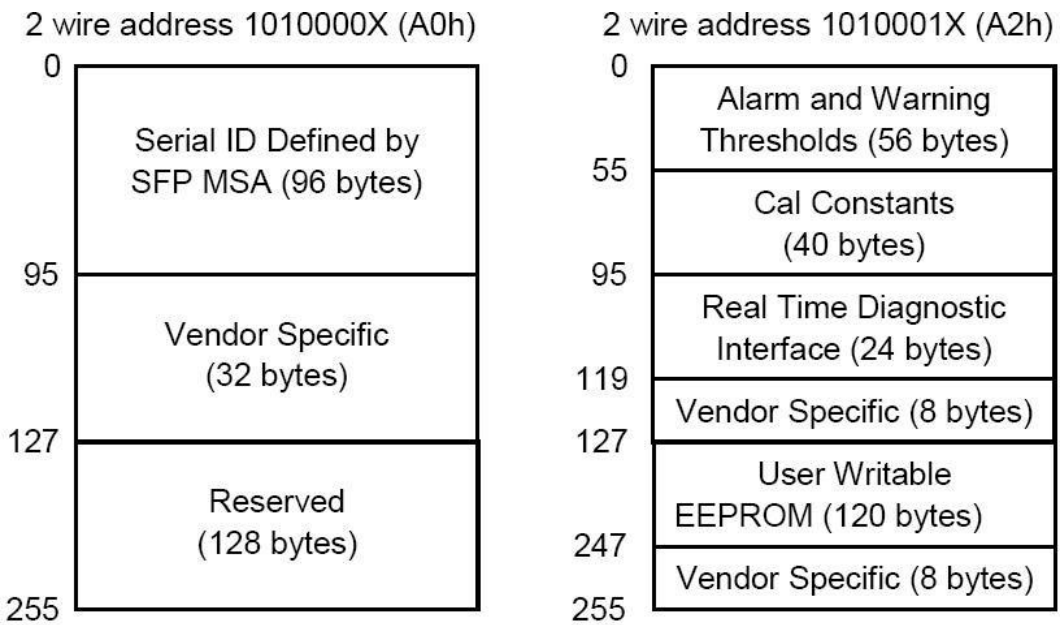
Parameter	Range	Unit	Accuracy	Calibration
Temperature	0 to +70	° C	±5° C	Internal/External
Voltage	3.0 to 3.6	V	±3%	Internal/External
Bias Current	0 to 20	mA	±10%	Internal/External
TX Power	-8 to 3	dBm	±3dB	Internal/External
RX Power	-14 to 0	dBm	±3dB	Internal/External

Digital Diagnostic Memory Map

The transceivers provide serial ID memory contents and diagnostic information about the present operating conditions by the 2-wire serial interface (SCL, SDA).

The diagnostic information with internal calibration or external calibration all are implemented, including received power monitoring, transmitted power monitoring, bias current monitoring, supply voltage monitoring and temperature monitoring.

The digital diagnostic memory map specific data field defines as following..



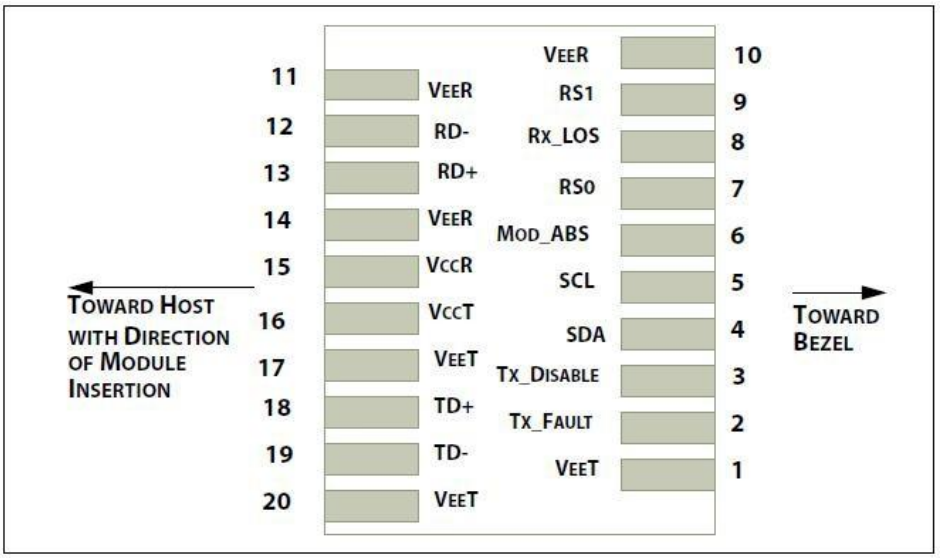
VI. Pin Descriptions

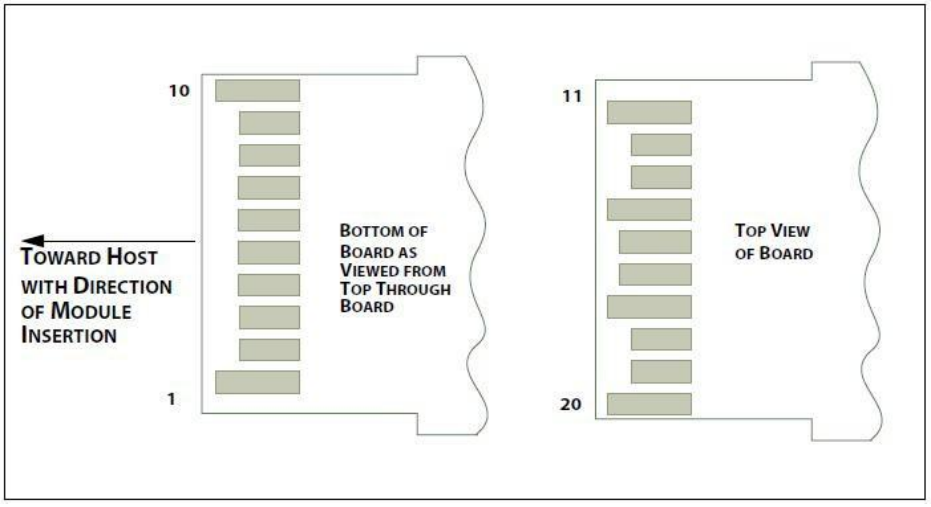
PIN	Logic	Symbol	Name/Description	Note
1		VeeT	Module Transmitter Ground	1
2	LVTTL-O	TX_Fault	Module Transmitter Fault	2
3	LVTTL-I	TX_Dis	Transmitter Disable; Turns off transmitter laser output	
4	LVTTL-I/O	SDA	2-Wire Serial Interface Data Line	
5	LVTTL-I	SCL	2-Wire Serial Interface Clock	
6		MOD_ABS	Module Definition, Grounded in the module	
7	LVTTL-I	RS0	Receiver Rate Select	
8	LVTTL-O	RX_LOS	Receiver Loss of Signal Indication Active LOW	
9	LVTTL-I	RS1	Transmitter Rate Select (not used)	
10		VeeR	Module Receiver Ground	1
11		VeeR	Module Receiver Ground	1
12	CML-O	RD-	Receiver Inverted Data Output	
13	CML-O	RD+	Receiver Data Output	
14		VeeR	Module Receiver Ground	1
15		VccR	Module Receiver 3.3 V Supply	
16		VccT	Module Receiver 3.3 V Supply	
17		VeeT	Module Transmitter Ground	1
18	CML-I	TD+	Transmitter Non-Inverted Data Input	
19	CML-I	TD-	Transmitter Inverted Data Input	
20		VeeT	Module Transmitter Ground	1

Notes:

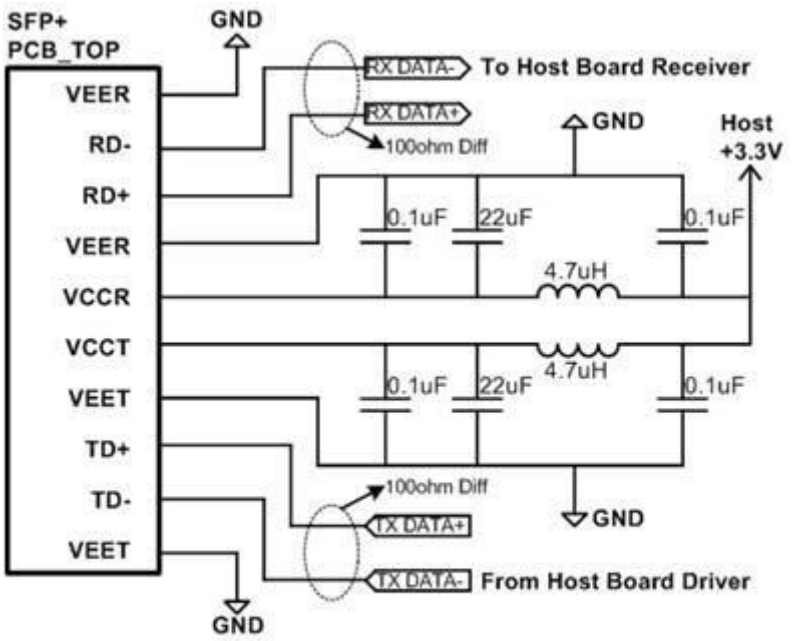
1. Module ground pins GND are isolated from the module case.

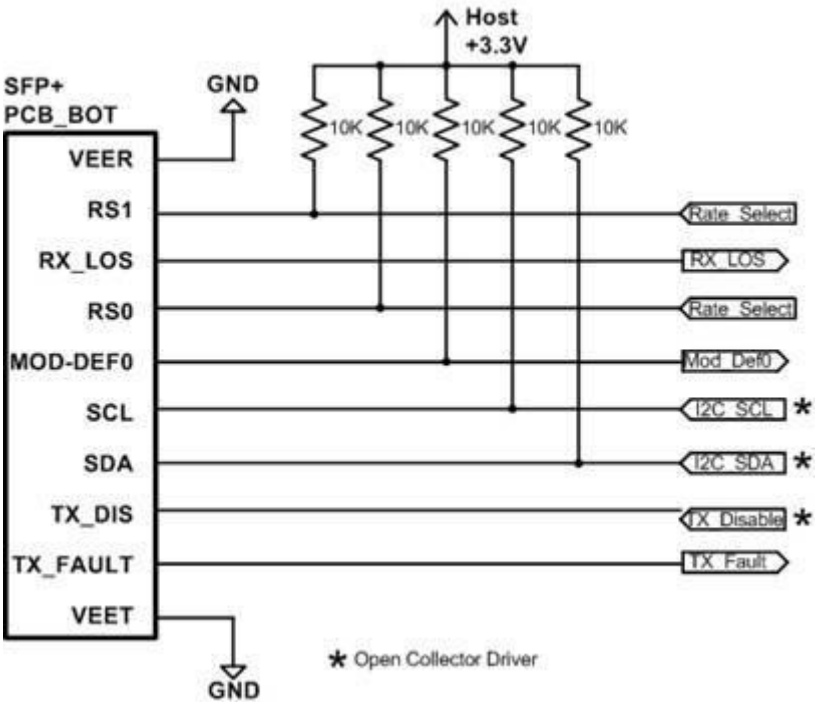
2. Shall be pulled up with 4.7K-10Kohms to a voltage between 3.15V and 3.45V on the host board..


11
VEER
12
RD-
13
RD+
14
VEER
15
VCCR
16
VCCT
17
VEET
18
TD+
19
TD-
20
VEET
TOWARD HOST WITH DIRECTION OF MODULE INSERTION
VEER
10
RS1
9
RX_LOS
8
RS0
7
MOD_ABS
6
SCL
5
SDA
4
TX_DISABLE
3
TX_FAULT
2
VEET
1
TOWARD BEZEL


10
1
TOWARD HOST WITH DIRECTION OF MODULE INSERTION
BOTTOM OF BOARD AS VIEWED FROM TOP THROUGH BOARD
11
20
TOP VIEW OF BOARD

VII. Recommended Interface Circuit





VIII. Mechanical Dimensions