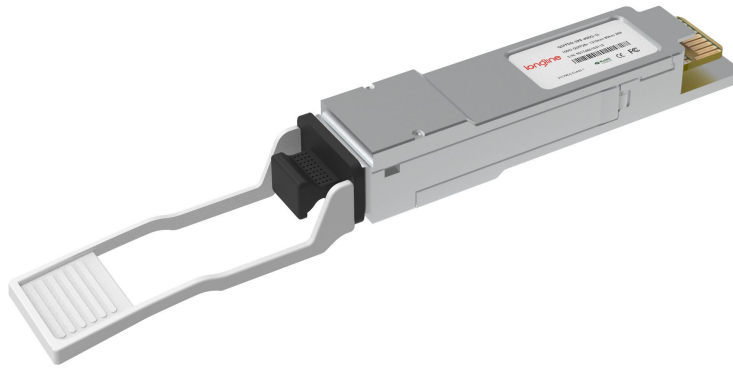


QSFP-DD 400GBASE-SR8 850nm 100m Transceiver

QSFDD-SR8-400G-LL



Application

- 400GBASE-SR8 400G Ethernet
- Data Center

Features

- Hot pluggable QSFP-DD form factor
- Supports 400Gb/s aggregate bit rate
- Up to 53.125Gbps data rate per channel
- Maximum link length of 70m on OM3 and 100m on OM4
- MPO connector receptacle
- Case temperature range: 0 ~ +70°C
- Power dissipation: <10W
- Single 3.3V power supply
- Compliant to QSFP-DD MSA
- Compliant with IEEE 802.3cd
- RoHS complaint

Description

This is a hot-pluggable QSFP-DD transceiver for 400G links over multimode fiber. It is a high performance module for short-range data communication and interconnect application which operates at 400Gbps up to 70m using OM3 multimode fiber or 100m using OM4 multimode fiber. This module is designed to operate over multimode fiber systems using a nominal wavelength of 850nm. The electrical interface uses a 76 pins connector. The optical interface uses MPO connector.

Product Specifications

I. Absolute Maximum Ratings

It has to be noted that the operation in of any individual absolute maximum ratings might cause permanent damage to this module.

Parameter	Symbol	Min	Typ.	Max	Unit	Ref.
Storage Temperature	Ts	-40		+85	°C	
Operating Humidity	RH	5		85	%	
Supply Voltage	Vcc	-0.4		3.6	V	

II. Recommended Operating Environment

Recommended Operating Environment specifies parameters for which the electrical and optical characteristics hold unless otherwise noted.

Parameter	Symbol	Min	Typ.	Max	Unit	Ref.
Operating Case Temperature	Tc	0		+70	°C	
Supply Voltage	Vcc	3.135	3.3	3.465	V	
Supply Current	Icc			2730	mA	
Bit Rate	BR		400		Gbps	
Fiber Length on OM3 MMF				70	m	
Fiber Length on OM4 MMF				100	m	

III. Optical Characteristics

Parameter	Symbol	Min	Typ.	Max	Unit	Ref.
Transmitter						
Modulation Format	PAM4					
Signaling Rate, each lane (range)	26.5625±100ppm				GBd	
Center Wavelength	λ_0	840		860	nm	
Spectral Width (RMS)	σ			0.6	nm	1
Average Launch Power, each lane		-6		4	dBm	
Outer Optical Modulation Amplitude (OMA_{outer}), each lane (max)				3	dBm	
Outer Optical Modulation Amplitude (OMA_{outer}), each lane (min)		-4.0			dBm	2
Launch power in OMA_{outer} minus TDECQ (min)		-5.9			dBm	
Transmitter and dispersion eye closure (TDECQ), each lane (max)	TDECQ			4.9	dBm	
Average launch power of OFF transmitter, each lane (max)				-30	dBm	
Extinction Ratio, each lane	ER	3			dB	
Optical Return Loss Tolerance	ORL			12	dB	
Receiver						
Modulation Format	PAM4					

Signaling Rate, each lane (range)			26.5625 ± 100 ppm		GBd	
Receiver Wavelength	λ	840		860	nm	
Damage Threshold(min)		5			dBm	3
Average Receive Power, each lane (max)				4	dBm	
Average Receive Power, each lane (min)		-7.9			dBm	4
Receive Power, each lane (OMA_{outer}) (max)				3	dBm	
Receiver Reflectance	R _r			-12	dB	
Stressed Receiver Sensitivity (OMA), each lane	R _{SENS}			-3	dBm	
Receiver Sensitivity (OMA_{outer}), each lane (max)			RS = max (-6.5 , SECQ - 7.9)		dB	5
Conditions of Stressed Receiver Sensitivity Test:						
Stressed Eye Closure for PAM4 (SECQ), lane under test			4.9		dB	6
OMA_{outer} of Each Aggressor Lane			3		dBm	6

Notes:

- 1.RMS spectral width is the standard deviation of the spectrum.
- 2.Even if the TDECQ < 1.9 dB, the OMA (min) must exceed this value.
- 3.The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level on one lane. The receiver does not have to operate correctly at this input power.
- 4.Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
- 5.Receiver sensitivity is informative and is defined for a transmitter with a value of SECQ.
- 6.These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

IV. Electrical Characteristics

The following electrical characteristics are defined over the Recommended Operating Environment unless otherwise specified.

Parameter	Symbol	Min	Typ.	Max	Unit	Ref.
Supply Voltage	Vcc	3.135	3.3	3.465	V	
Supply Current	Icc			2730	mA	
Transmitter						
Input Differential Impedance	Rin		100		Ω	1
Differential Data Input Swing	Vin,pp	400		900	mV	
Receiver						
Differential data output swing	Vout,pp			900	mV	2

Notes:

- 1.Connected directly to TX data input pins.
- 2.In to 100Ω differential termination.

V. Digital Diagnostic Monitoring Information

The following digital diagnostic characteristics are defined over the normal operating conditions unless otherwise specified.

Parameter	Accuracy	Calibration	Ref.
Temperature	±3°C	Internal	
Voltage	±3%	Internal	
Bias Current	±10%	Internal	
TX Power	±3dB	Internal	
RX Power	±3dB	Internal	

VI. Pin Assignment

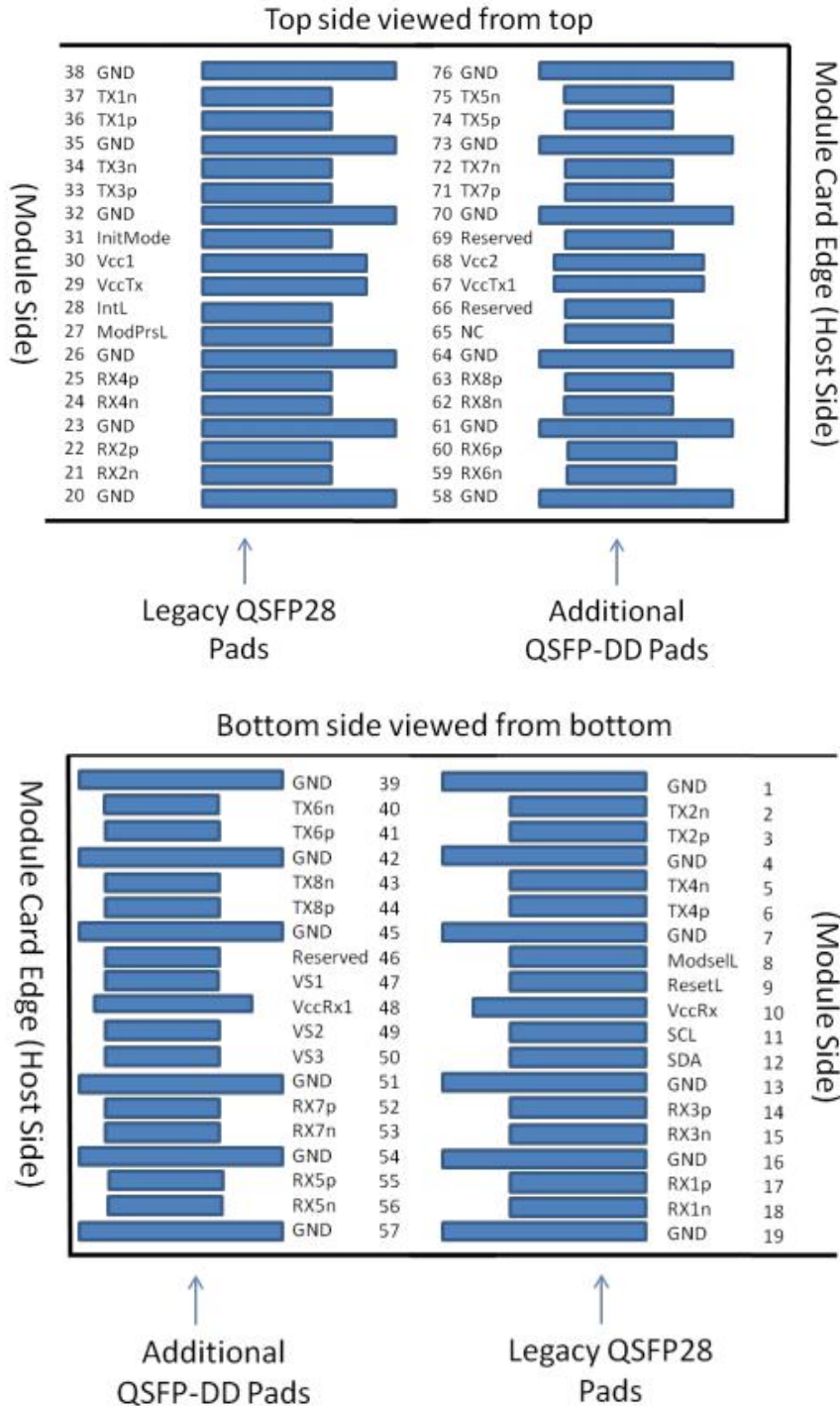


Figure 1 – QSFP-DD Pin Assignment

Pin	Logic	Symbol	Description	Plug Sequence ⁴	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTTL-I	ModSelL	Module Select	3B	
9	LVTTTL-I	ResetL	Module Reset	3B	
10		VccRx	+3.3 V Power Supply Receiver	2B	2
11	LVC MOS-I/O	SCL	2-wire serial interface clock	3B	
12	LVC MOS-I/O	SDA	2-wire serial interface data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	

26		GND	Ground	1B	1
27	LVTTTL-O	ModPrsL	Module Present	3B	
28	LVTTTL-O	IntL	Interrupt	3B	
29		VccTx	+3.3V Power supply transmitter	2B	2
30		Vcc1	+3.3V Power supply	2B	2
31	LVTTTL-I	InitMode	Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1
39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Output	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Output	3A	
45		GND	Ground	1A	1
46		Reserved	For future use	3A	3
47		VS1	Module Vendor Specific 1	3A	3
48		VccRx1	3.3V Power Supply	2A	2

49		VS2	Module Vendor Specific 2	3A	3
50		VS3	Module Vendor Specific 3	3A	3
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reseved	For future use	3A	3
67		VccTx1	3.3V Power Supply	2A	2
68		Vcc2	3.3V Power Supply	2A	2
69		Reseved	For future use	3A	3
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Output	3A	

72	CML-I	Tx7n	Transmitter Inverted Data Output	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Output	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Output	3A	
76		GND	Ground	1A	1

Notes:

1. QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground plane.
2. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 6. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.
3. All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 Kohms and less than 100 pF.
4. Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (see Figure 2 for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A, 1B will then occur simultaneously, followed by 2A, 2B, followed by 3A, 3B.

VII. Optical Module Block Diagram

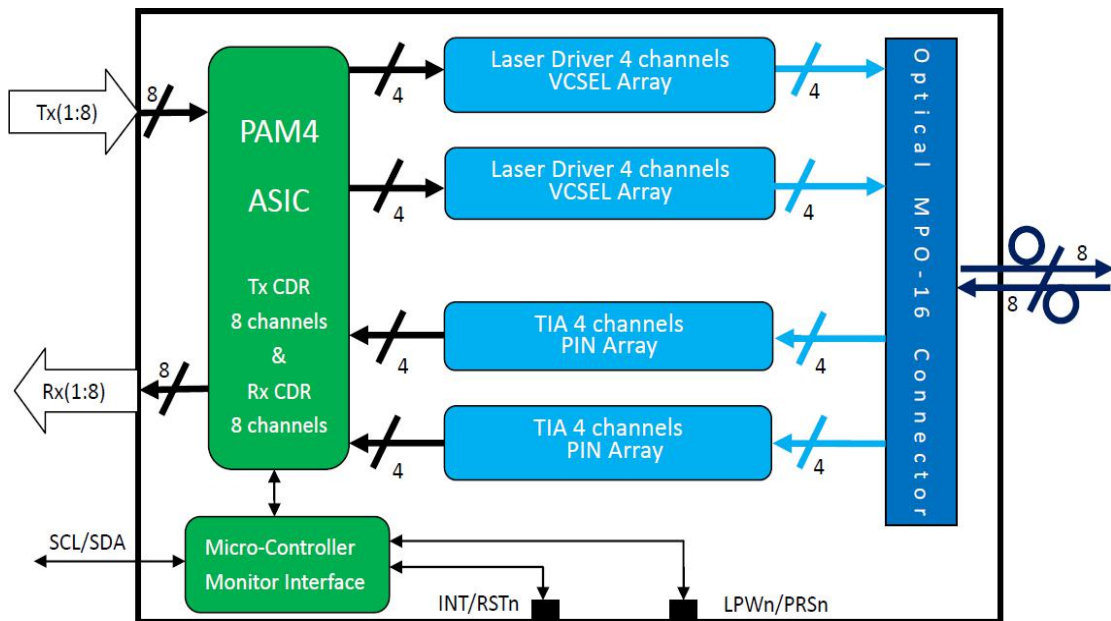
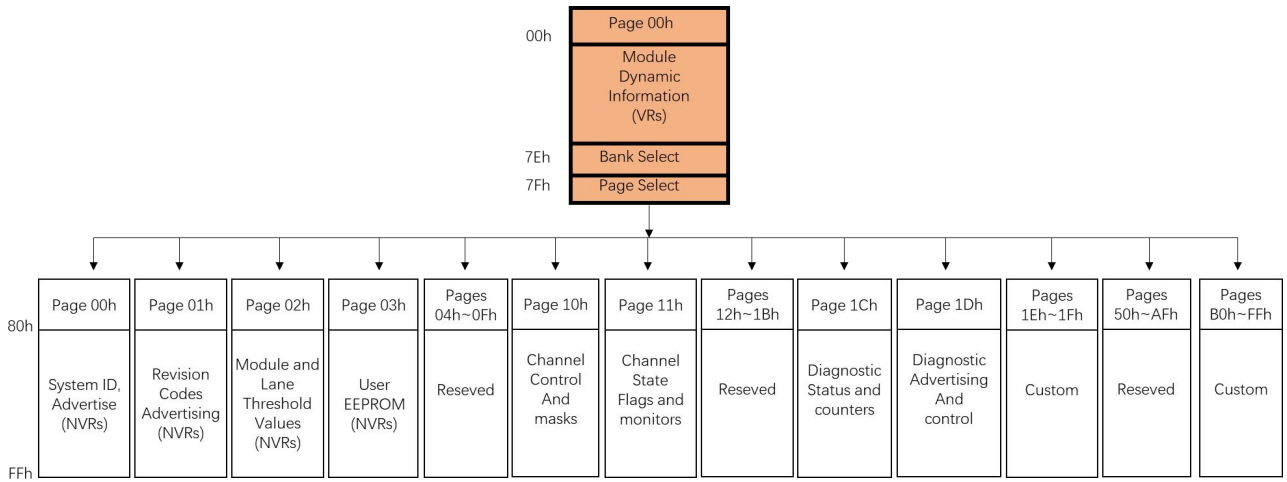


Figure 2. Transceiver Block Diagram

VIII. EEPROM Memory Map

CMIS Module Memory Map:



Digital Interface:

Table-Lower Page Overview

Address	Size	Name	Description
0-1	2	Id and version ID	Module ID from SFF-8024 list, version number, Type and status
2-3	2	Flat mem, CLEI present, TWI speed, Module State, Interrupt	Flat mem indication, CLEI present indicator, Maximum TWI speed, Current state of Module, Current state of the Interrupt signal
4-7	4	Bank Lane Flag Summary	Flag summary of all lane flags on pages 10h-1Fh
8-13	6	Module Flags	All flags that are module wide (i.e.not lane specific)
14-25	12	Module Monitors	
26-30	5	Module Global Controls	
31-36	6	Module masks	Module flag masks
37-63	27	Reserved	
64-84	21	Custom	
85	1	Module Type advertising code	
86-117	32	Module Host-Media Interface Advertising Options	Host and media interfaces that are supported by the module

118-125	8	Password area	
126	1	Bank Select Byte	
127	1	Page Select Byte	

Table-Upper Page 00 Overview

Address	Size	Name	Description
128	1	Identifier	Identifier Type of module
129-144	16	Vendor name	Vendor name(ASCII)
145-147	3	Vendor OUI	Vendor IEEE company ID
148-163	16	Vendor PN	Part number provided by vendor (ASCII)
164-165	2	Vendor rev	Revision level for part number provided by vendor (ASCII)
166-181	16	Vendor SN	Vendor Serial Number (ASCII)
182-189	8	Date Code	
190-199	10	CLEI code	Common Language Equipment Identification code
200-201	2	Module power characteristics	
202	1	Cable assembly length	
203	1	Media Connector Type	
204-209	6	Copper Cable Attenuation	
210-211	2	Cable Assembly Lane Information	
212	1	Media Interface Technology	
213-220	8	Reserved	
221	1	Custom	
222	1	Checksum	Includes bytes 128-221
223-255	33	Custom Info NV	

Table-Upper Page 01 Overview

Byte	Size	Name	Description
128-131	4	Module Firmware and Hardware revisions	
132-137	6	Supported link length	Supported lengths of various fiber media
138-139	2	Nominal Wavelength	
140-141	2	Wavelength Tolerance	
142-144	3	Implemented Management Interface features advertising	
145-154	10	Module Characteristics advertising	
155-156	2	Implemented Controls advertising	
157-158	2	Implemented Flags advertising	
159-160	2	Implemented Monitors advertising	
161-162	2	Implemented Signal Integrity Controls advertising	
163-175	13	Reserved	
176-190	15	Module Media Lane advertising	
191-222	32	Custom	
223-250	28	Extended Module Host-Media Interface Advertising options	
251-254	4	Reserved	
255	1	Checksum	Checksum of bytes 130-254 ¹

Table-Upper Page 02 Overview

Byte	Size	Name	Description
128-175	48	Module-level monitor thresholds	
176-199	24	Lane-specific monitor thresholds	
200-229	30	Reserved	
230-254	25	Customizable space	
255	1	Checksum	Covers bytes 128-254

Table-Upper Page 16 Overview

Byte	Size	Name	Description
128	1	Data Path Power control	Data Path Pwr Up bits for each lane, controls Data Path State machine
129-142	14	Lane-Specific Control	Fields to control lane attributes independent of the Data Path State machine or control sets
143-177	35	Staged Control Set 0	Fields to configure the selected Application Code and signal integrity settings
178-212	35	Staged Control Set 1	Fields to configure the selected Application Code and signal integrity settings
213-231	19	Lane-Specific Flag Masks	
232-239	8	Reserved	
240-255	16	Custom	

Table-Upper Page 17 Overview

Byte	Size	Name	Description
128-131	4	Datapath State indicators	
132-133	5	Reserved	
134-152	19	Lane-specific flags	
153	1	Reserved	
154-201	48	Lane-specific monitors	
202-205	4	Configuration Error Codes	Indicates validity of select Application codes
206-234	29	Active Control Set	
235-239	5	Reserved	
240-255	16	Host Electrical to Module Media Lane Mapping	Indicates the mapping of Host Electrical lanes to Module Media lanes

IX. Diagram Mechanical Drawing

Dimensions are in millimeters. (Unit: mm)

