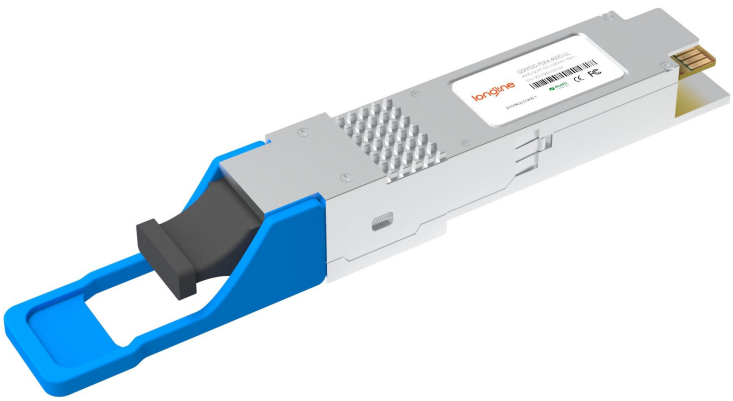
400G-PLR4 QSFPDD 1310nm 10km MTP/MPO Transceiver for SMF

QSFPDD-PLR4-400G-LL



Application

- Data Center Interconnect
- 400G Ethernet
- Infiniband Interconnect
- Enterprise Networking

Features

- Maximum Power Consumption 10W
- Case Operating Temperature 0℃ to 70℃
- Two Wire Serial Interface with Digital Diagnostic Monitoring
- Class 1 Laser
- Compliant with QSFP-DD MSA HW Rev 5.0 Type 2 Housing with MPO-12 Connector
- Compliant with QSFP-DD CMIS Rev 4.0
- Compliant with EU Directive 2011/65/EU (RoHS Compliant)
- Compliant with IEEE802.3bs Standard: 400GAUI-8 Electrical Interface
- Compliant with IEEE802.3cu Standard: 4x100GBASE-LR1 Optical Interface

Description

This product is a 400Gb/s Quad Small Form Factor Pluggable-double density (QSFP-DD) optical module designed for 10km optical communication applications. The product is designed with form factor, optical/electrical connection and digital diagnostic interface according to the QSFP-DD Multi- Source Agreement (MSA).

Product Specifications

I. Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Notes
Storage Temperature Range	Ts	-40	85	℃	
Relative Humidity (Non-condensing)	RH	5	95	%	
Supply Voltage	V_{CC}	-0.5	3.6	V	
Control Input Voltage	V_I	-0.3	V_{CC}+0.5	V	

II. Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Operating Case Temperature	T_{OPR}	0		70	℃	
Power Supply Voltage	V_{CC}	3.135	3.3	3.465	V	
Instantaneous Peak Current at Hot Plug	I_{CC_IP}			4000	mA	
Sustained Peak Current at Hot Plug	I_{CC_SP}			3300	mA	
Maximum Power Dissipation	P_D			10	W	
Maximum Power Dissipation, Low Power Mode	P_{DLP}			1.5	W	

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Signalling Rate Per Lane	SRL		53.125		GBd	PAM4
Two Wire Serial Interface Clock Rate				400	kHz	
Power Supply Noise Tolerance (10Hz-10MHz)				66	mV	
Rx Differential Data Output Load			100		Ohm	
Operating Distance		2		10000	m	

III. Electrical Characteristics Low Speed Signal

Parameter	Symbol	Min.	Max.	Unit	Condition
Module Output SCL and SDA	V_{OL}	0	0.4	V	
Module Input SCL and SDA	V_{IL}	-0.3	V_{CC}*0.3	V	
	V_{IH}	V_{CC}*0.7	V_{CC}+0.5	V	
InitMode, ResetL and ModSelL	V_{IL}	-0.3	0.8	V	
	V_{IH}	2	V_{CC}+0.3	V	
IntL	V_{OL}	0	0.4	V	
	V_{OH}	V_{CC}-0.5	V_{CC}+0.3	V	

IV. Electrical Characteristics High Speed Signal

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Transmitter Electrical Characteristics						
Differential Pk-pk Input Voltage Tolerance		900			mV	
Differential Termination Mismatch				10	%	
Single-ended Voltage to Lerance Range		-0.4		3.3	V	
DC Common Mode Voltage		-350		2850	mV	
Receiver Electrical Characteristics						
AC Common-mode Output Voltage (RMS)				17.5	mV	
Differential Output Voltage				900	mV	
Near-end Eyeheight, Differential		70			mV	
Far-end Eyeheight, Differential		30			mV	
Farend Pre-cursor Ratio		-4.5		2.5	%	
Differential Termination Mismatch				10	%	
Transition Time (Min, 20% to 80%)		9.5			ps	
DC Common Mode Voltage		-350		2850	mV	

V. Optical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Transmitter Optical Characteristics						
Wavelength	λ_C	1304.5	1311	1317.5	nm	
Side Mode Suppression Ratio	SMSR	30			dB	
Average Launch Power, Each Lane	AOP_L	-1.9		4.8	dBm	1
Outer Optical Modulation Amplitude (OMA_{outer}), Each Lane	T_{OMA}			5	dBm	
Outer Optical Modulation Amplitude (OMA_{outer}), Each Lane: for TDECQ <1.4dB for 1.4≤TDECQ≤3.4dB	T_{OMA}	1.1 -0.3+TDECQ			dBm	
Transmitter and Dispersion Eye Closure for PAM4(TDECQ), Each Lane	TDECQ			3.4	dB	
Transmitter Eye Closure for PAM4(TECQ)	TECQ			3.4	dB	
|TDECQ-TECQ|				2.5	dB	
Over/Under-shoot				22	%	
Transmitter Power Excursion				2.8	dBm	
Average Launch Power of OFF Transmitter, Each Lane	T_{OFF}			-15	dBm	
ExtinctionRatio, Each Lane	ER	3.5			dB	
$RIN_{15.6}OMA$	RIN			-136	dB/Hz	
Optical Return Loss Tolerance	ORL			15.6	dB	
Transmitter Reflectance	T_R			-26	dB	
Transmitter Transition Time	Tt			17	ps	

Parameter	Symbol	Unit	Min.	Typ.	Max.	Notes
Receiver Optical Characteristics						
Wavelength	λ_C	1304.5	1311	1317.5	nm	
Damage Threshold, Each Lane	AOP_D	5.8			dBm	
Average Receive Power, Each Lane	AOP_R	-8.2		4.8	dBm	2
Receive Power(OMA_{outer}), Each Lane	OMA_R			5	dBm	
Receiver Reflectance	RR			-26	dB	
Receiver Sensitivity(OMA_{outer}), Each Lane for TECQ<1.4dB for1.4≤TECQ≤3.4dB	S_{OMA}			-6.1 -7.5+TECQ	dBm	
Stressed Receiver Sensitivity(OMA_{outer}), Each Lane	SRS			-4.1	dBm	3
Conditions of Stressed Receiver Sensitivity Test						
Stressed Eye Closure for PAM4(SECQ)			3.4		dB	

Notes:

1. Average launch power, each lane (min) is informative and not the principal indicator of signal strength.
2. Average receive power, (min) is informative and not the principal indicator of signal strength.
3. Measured with conformance test signal at TP3 for the BER = 2.4x10-4.

VI. Pin Function Definitions

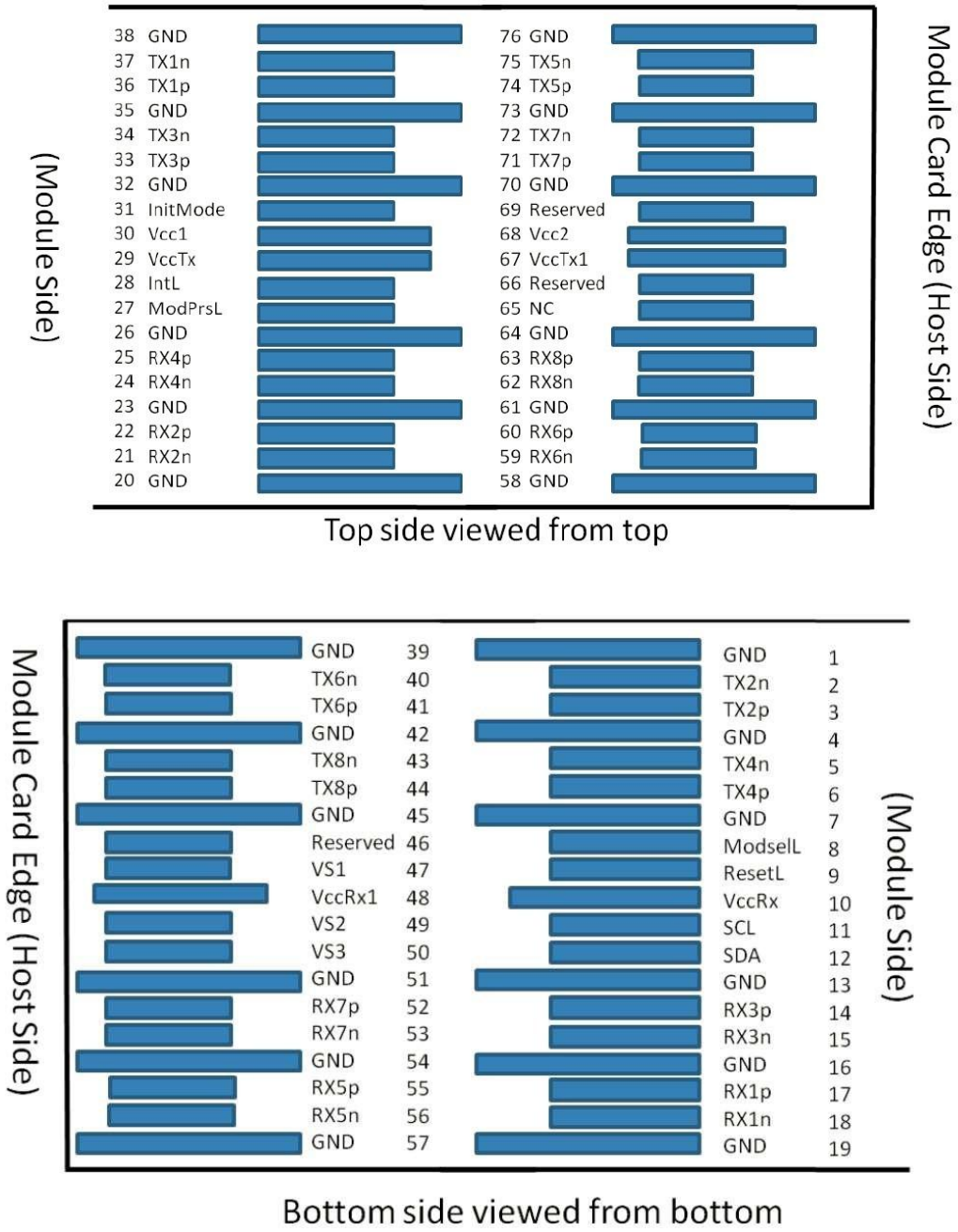


Figure1. Pin Definitions of the Module High Speed Inputs/Outputs

VII. Transceiver Pin Descriptions

Pin No.	Logic	Symbol	Definition
1		GND	Ground
2	CML-I	Tx2n	Transmitter Inverted Data Input
3	CML-I	Tx2p	Transmitter Non-inverted Data Input
4		GND	Ground
5	CML-I	Tx4n	Transmitter Inverted Data Input
6	CML-I	Tx4p	Transmitter Non-inverted Data Input
7		GND	Ground
8	LVTTL-I	ModSelL	Module Select
9	LVTTL-I	ResetL	Module Reset
10		V_{cc}Rx	+3.3V Power Supply Receiver
11	LVCMOS-I/O	SCL	2-wire Serial Interface Clock
12	LVCMOS-I/O	SDA	2-wire Serial Interface Data
13		GND	Ground
14	CML-O	Rx3p	Receiver Non-inverted Data Output
15	CML-O	Rx3n	Receiver Inverted Data Output
16		GND	Ground

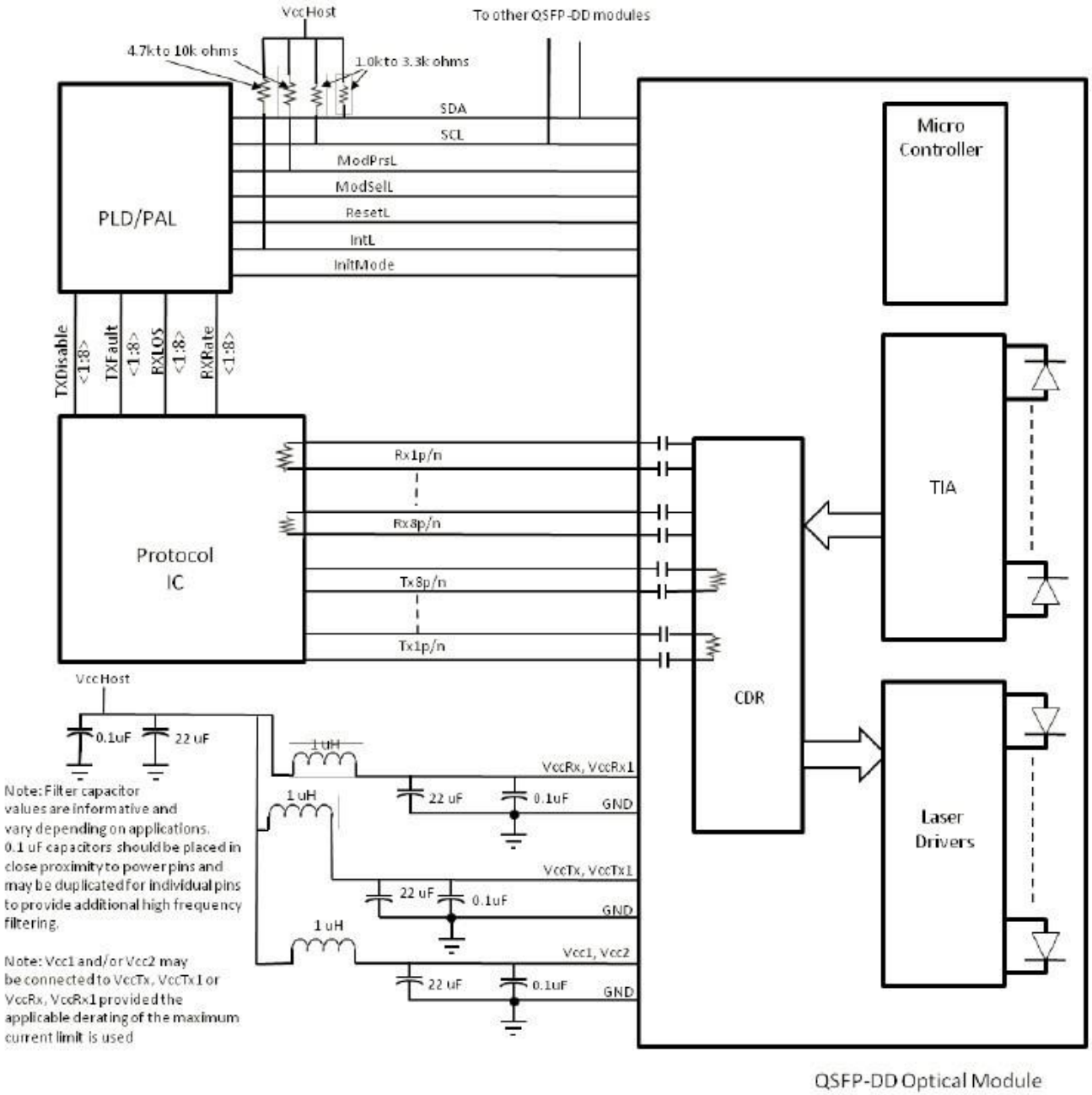
Pin No.	Logic	Symbol	Definition
17	CML-O	Rx1p	Receiver Non-inverted Data Output
18	CML-O	Rx1n	Receiver Inverted Data Output
19		GND	Ground
20		GND	Ground
21	CML-O	Rx2n	Receiver Inverted Data Output
22	CML-O	Rx2p	Receiver Non-inverted Data Output
23		GND	Ground
24	CML-O	Rx4n	Receiver Inverted Data Output
25	CML-O	Rx4p	Receiver Non-inverted Data Output
26		GND	Ground
27	LVTTL-O	ModPrsL	Module Present
28	LVTTL-O	IntL	Interrupt
29		V_{cc} Tx	+3.3V Power Supply Transmitter
30		V_{cc} 1	+3.3V Power Supply
31	LVTTL-I	InitMode	Initialization Mode
32		GND	Ground

Pin No.	Logic	Symbol	Definition
33	CML-I	Tx3p	Transmitter Non-inverted Data Input
34	CML-I	Tx3n	Transmitter Inverted Data Input
35		GND	Ground
36	CML-I	Tx1p	Transmitter Non-inverted Data Input
37	CML-I	Tx1n	Transmitter Inverted Data Input
38		GND	Ground
39		GND	Ground
40	CML-I	Tx6n	Transmitter Inverted Data Input
41	CML-I	Tx6p	Transmitter Non-inverted Data Input
42		GND	Ground
43	CML-I	Tx8n	Transmitter Inverted Data Input
44	CML-I	Tx8p	Transmitter Non-inverted Data Input
45		GND	Ground
46		Reserved	
47		VS1	Module Vendor Specific 1
48		V_{cc} Rx1	3.3V Power Supply

Pin No.	Logic	Symbol	Definition
49		VS2	Module Vendor Specific 2
50		VS3	Module Vendor Specific 3
51		GND	Ground
52	CML-O	Rx7p	Receiver Non-inverted Data Output
53	CML-O	Rx7n	Receiver Inverted Data Output
54		GND	Ground
55	CML-O	Rx5p	Receiver Non-inverted Data Output
56	CML-O	Rx5n	Receiver Inverted Data Output
57		GND	Ground
58		GND	Ground
59	CML-O	Rx6n	Receiver Inverted Data Output
60	CML-O	Rx6p	Receiver Non-inverted Data Output
61		GND	Ground
62	CML-O	Rx8n	Receiver Inverted Data Output
63	CML-O	Rx8p	Receiver Non-inverted Data Output
64		GND	Ground

Pin No.	Logic	Symbol	Definition
65		NC	Not Connected
66		Reserved	
67		V_{cc} Tx1	3.3V Power Supply
68		V_{cc} 2	3.3V Power Supply
69		Reserved	
70		GND	Ground
71	CML-I	Tx7p	Transmitter Non-inverted Data Input
72	CML-I	Tx7n	Transmitter Inverted Data Input
73		GND	Ground
74	CML-I	Tx5p	Transmitter Non-inverted Data Input
75	CML-I	Tx5n	Transmitter Inverted Data Input
76		GND	Ground

VIII. Block Diagram



IX. Package Outline