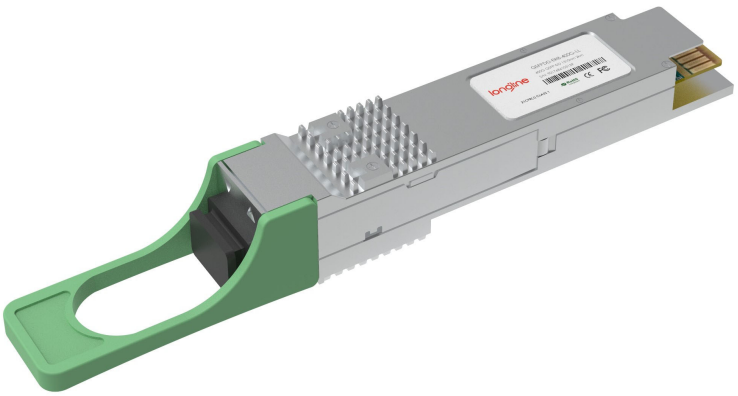
400GBASE-ER8 QSFP-DD PAM4 1310nm 40km LC SMF DOM Optical Transceiver Module

QSFPDD-ER8-400G-LL



Application

- 400GBASE-ER8 400G Ethernet
- Data Center
- Telecom
- 40km Transmission on Single Mode Fiber

Features

- Compliant with IEEE std 802.3cnTM-2019:
  -400GBASE-ER8 optical interface
  -400GAUI-8 electrical interface
- Compliant with QSFP-DD MSA HW Rev 5.0 with duplex LC connector
- Compliant with QSFP-DD CMIS Rev 4.0
- Two wire serial Interface with digital diagnostic monitoring
- Class 1/1M Laser
- Complies with EU Directive 2011/65/EU (RoHS compliant)
- Operating case temperature: 0℃ to 70℃

Product Specifications

I. Absolute Maximum Ratings

It has to be noted that the operation in of any individual absolute maximum ratings might cause permanent damage to this module.

Parameter	Symbol	Min.	Max.	Unit	Notes
Storage Temperature	T_S	-40	85	ºC	
Supply Voltage	V_{cc}	-0.5	3.6	V	
Relative Humidity (non-condensing)	RH	5	95	%	
Data Input Voltage Differential	$\|V_{DIP}-V_{DIN}\|$	-	1	V	
Control Input Voltage	V_I	-0.3	Vcc+0.5	V	
Control Output Current	I_O	-20	20	mA	

II. Recommended Operating Environment

Electrical and optical characteristics below are defined under this operating environment, un- less otherwise specified.

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Operating Case Temperature	T_{OPR}	0	-	70	ºC	
Power Supply Voltage	V_{cc}	3.135	3.3	3.465	V	
Instantaneous peak current at hot plug	I_{CC_IP}	-	-	5600	mA	
Sustained peak current at hot plug	I_{CC_SP}	-	-	4620	mA	
Maximum Power Dissipation	P_D	-	-	14	W	
Maximum Power Dissipation, Low Power Mode	P_{DLP}	-	-	1.5	W	
Signalling Speed per Lane	DRL	-	26.5625	-	GBd	
Control Input Voltage High	V_{IH}	Vcc*0.7	-	Vcc+0.3	V	
Control Input Voltage Low	V_{IL}	-0.3	-	Vcc*0.3	V	
Two Wire Serial Interface Clock Rate	-	-	-	400	kHz	
Power Supply Noise	-	-	-	66	mVpp	
Rx Differential Data Output Load	-	-	100	-	Ohm	
Operating Distance	-	0.002	-	40	km	1

Note 1: Channel insertion loss is 18dB for 40km.

III. Functional Characteristics (Optical)

The following tables list the performance specifications for the various functional blocks of the integrated optical transceiver module.

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Transmitter						
Wavelength L0	λ_{C0}	1272.55	1273.55	1274.54	nm	
Wavelength L1	λ_{C1}	1276.89	1277.89	1278.89	nm	
Wavelength L2	λ_{C2}	1281.25	1282.26	1283.27	nm	
Wavelength L3	λ_{C3}	1285.65	1286.67	1287.68	nm	
Wavelength L4	λ_{C4}	1294.53	1295.56	1296.59	nm	
Wavelength L5	λ_{C5}	1299.02	1300.06	1301.09	nm	
Wavelength L6	λ_{C6}	1303.54	1304.59	1305.63	nm	
Wavelength L7	λ_{C7}	1308.09	1309.14	1310.19	nm	
Side Mode Suppression Ratio	SMSR	30	-	-	dB	
Total Average Launch Power	AOP_T	-	-	14.6	dBm	
Average Launch Power, each lane	AOP_L	-0.6	-	5.6	dBm	1
Outer Optical Modulation Amplitude (OMAouter),each Lane	T_{OMA}	2.4	-	6.4	dBm	
Difference in Launch Power between any two Lanes(OMAouter)	D_{T_OMA}	-	-	4	dB	
Launch Power in OMAouter minus TDECQ,each lane	$T_{OMA-TDECQ}$	1	-	-	dBm	
Transmitter and Dispersion Eye Closure for PAM4(TDECQ), each lane	TDECQ	-	-	3.4	dB	
TDECQ –10log10(Ceq)	-	-	-	3.4	dB	
Average Launch Power of OFF Transmitter,each lane	T_{OFF}	-	-	-30	dBm	
Extinction Ratio	ER	6	-	-	dB	
RIN15OMA	RIN	-	-	-132	dB/Hz	
Optical Return Loss Tolerance	ORL	-	-	15	dB	
Transmitter Reflectance	T_R	-	-	-26	dB	2

Note 1: Average launch power, each lane (min) is informative and not the principal indicator of signal strength

Note 2: Transmitter reflectance is defined looking into the transmitter

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Receiver						
Wavelength L0	λ_{C0}	1272.55	1273.55	1274.54	nm	
Wavelength L1	λ_{C1}	1276.89	1277.89	1278.89	nm	
Wavelength L2	λ_{C2}	1281.25	1282.26	1283.27	nm	
Wavelength L3	λ_{C3}	1285.65	1286.67	1287.68	nm	
Wavelength L4	λ_{C4}	1294.53	1295.56	1296.59	nm	
Wavelength L5	λ_{C5}	1299.02	1300.06	1301.09	nm	
Wavelength L6	λ_{C6}	1303.54	1304.59	1305.63	nm	
Wavelength L7	λ_{C7}	1308.09	1309.14	1310.19	nm	
Damage Threshold, each Lane	AOP_D	-3.4	-	-	dBm	
Average Receive Power, each Lane	AOP_R	-18.6	-	-4.4	dBm	
Receive Power (OMAouter), each Lane	OMA_R	-	-	-3.6	dBm	
Difference in Receive Power between any twoLanes (OMAouter)	D_{R_OMA}	-	-	5.8	dB	
Receiver Reflectance	RR	-	-	-26	dB	
Receiver Sensitivity (OMAouter), each Lane	S_{OMA}	-	-	Max(–16.1, SECQ – 17.5)	dBm	1
Stressed Receiver Sensitivity (OMAouter),each Lane	SRS	-	-	-14.1	dBm	2
Conditions of stressed receiver sensitivity test:						
Stressed eye closure for PAM4 (SECQ), lane under test	-	-	3.4	-	dB	
SECQ – 10log10(Ceq), lane under test	-	-	-	3.4	dB	
OMAouter of each aggressor lane	-	-	-8.3	-	dBm	
Stressed eye closure for PAM4 (SECQ), lane under test	-	-	3.4	-	dB	

Note 1: Receiver sensitivity (OMAouter), each lane (max) is informative and is defined for a transmitter with SECQ of 1.4 dB.

Note 2: Measured with conformance test signal at TP3 for the BER = 2.4x10-4

IV. Electrical Characteristics

Electrical Specification High Speed Signal (compliant with IEEE 802.3 400GAUI-8)

Receiver (Module Output)

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
AC common-mode output Voltage (RMS)		-	-	17.5	mV	
Differential output Voltage		-	-	900	mV	
Near-end Eye height, differential		70	-	-	mV	
Far-end Eye height, differential		30	-	-	mV	
Far end pre-cursor ratio		-	-	2.5	%	
Differential Termination Mismatch		-	-	10	%	
Transition Time (min, 20% to 80%)		9.5	-	-	ps	
DC common mode Voltage		-350	-	2850	mV	

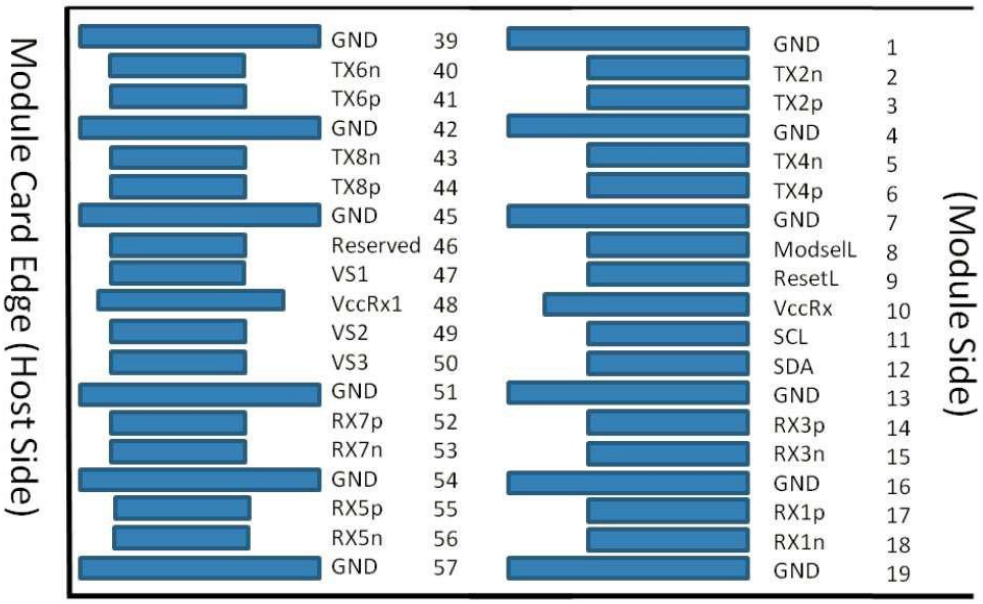
Transmitter (Module Input)

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Differential pk-pk input Voltage tolerance		900	-	-	mV	
Differential termination mismatch		-	-	10	%	
Single-ended voltage tolerance range		-0.4	-	3.3	V	
DC common mode Voltage		-350	-	2850	mV	

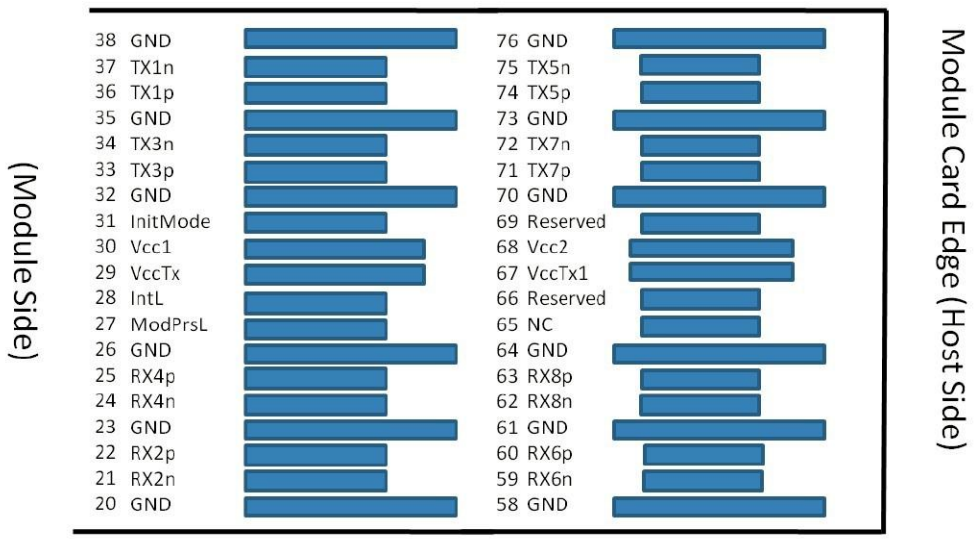
Electrical Specification Low Speed Signal (compliant with QSFP-DD HW Rev 5.1)

Parameter	Symbol	Min.	Typical	Max.	Unit
Module output SCL and SDA	V_{OL}	0	0.4	V	
Module Input SCL and SDA	V_{IL}	-0.3	V_{CC}*0.3	V	
	V_{IH}	V_{CC}*0.7	V_{CC}+0.5	V	
InitMode, ResetL and ModSelL	V_{IL}	-0.3	0.8	V	
	V_{IH}	2	V_{CC}+0.3	V	
IntL	V_{OL}	0	0.4	V	
	V_{OH}	V_{CC}-0.5	V_{CC}+0.3	V	

V. Pin Assignment



Bottom side viewed from bottom



Top side viewed from top

Pin definitions of the module high speed inputs/outputs

Pin #	Logic	Symbol	Definition	Pin #	Logic	Symbol	Definition
1		GND	Ground	39		GND	Ground
2	CML-I	Tx2n	Transmitter Inverted Data Input	40	CML-I	Tx6n	Transmitter Inverted Data Input
3	CML-I	Tx2p	Transmitter Non-inverted Data Input	41	CML-I	Tx6p	Transmitter Non-inverted Data Input
4		GND	Ground	42		GND	Ground
5	CML-I	Tx4n	Transmitter Inverted Data Input	43	CML-I	Tx8n	Transmitter Inverted Data Input
6	CML-I	Tx4p	Transmitter Non-inverted Data Input	44	CML-I	Tx8p	Transmitter Non-inverted Data Input
7		GND	Ground	45		GND	Ground
8	LVTTL-I	ModSelL	Module Select	46		Reserved	
9	LVTTL-I	ResetL	Module Reset	47		VS1	Module Vendor Specific 1
10		VccRx	+3.3V Power Supply Receiver	48		VccRx1	3.3V Power Supply
11	LVCMOS-I/O	SCL	2-wire serial interface clock	49		VS2	Module Vendor Specific 2
12	LVCMOS-I/O	SDA	2-wire serial interface data	50		VS3	Module Vendor Specific 3
13		GND	Ground	51		GND	Ground
14	CML-O	Rx3p	Receiver Non-inverted Data Output	52	CML-O	Rx7p	Receiver Non-inverted Data Output
15	CML-O	Rx3n	Receiver Inverted Data Output	53	CML-O	Rx7n	Receiver Inverted Data Output
16		GND	Ground	54		GND	Ground
17	CML-O	Rx1p	Receiver Non-inverted Data Output	55	CML-O	Rx5p	Receiver Non-inverted Data Output
18	CML-O	Rx1n	Receiver Inverted Data Output	56	CML-O	Rx5n	Receiver Inverted Data Output
19		GND	Ground	57		GND	Ground
20		GND	Ground	58		GND	Ground
21	CML-O	Rx2n	Receiver Inverted Data Output	59	CML-O	Rx6n	Receiver Inverted Data Output
22	CML-O	Rx2p	Receiver Non-inverted Data Output	60	CML-O	Rx6p	Receiver Non-inverted Data Output
23		GND	Ground	61		GND	Ground
24	CML-O	Rx4n	Receiver Inverted Data Output	62	CML-O	Rx8n	Receiver Inverted Data Output
25	CML-O	Rx4p	Receiver Non-inverted Data Output	63	CML-O	Rx8p	Receiver Non-inverted Data Output
26		GND	Ground	64		GND	Ground
27	LVTTL-O	ModPrsL	Module Present	65		NC	Not connected
28	LVTTL-O	IntL	Interrupt	66		Reserved	
29		VccTx	+3.3V Power Supply Transmitter	67		VccTx1	3.3V Power Supply
30		Vcc1	+3.3V Power Supply	68		Vcc2	3.3V Power Supply
31	LVTTL-I	InitMode	Initialization mode	69		Reserved	
32		GND	Ground	70		GND	Ground
33	CML-I	Tx3p	Transmitter Non-inverted Data Input	71	CML-I	Tx7p	Transmitter Non-inverted Data Input
34	CML-I	Tx3n	Transmitter Inverted Data Input	72	CML-I	Tx7n	Transmitter Inverted Data Input
35		GND	Ground	73		GND	Ground
36	CML-I	Tx1p	Transmitter Non-inverted Data Input	74	CML-I	Tx5p	Transmitter Non-inverted Data Input
37	CML-I	Tx1n	Transmitter Inverted Data Input	75	CML-I	Tx5n	Transmitter Inverted Data Input
38		GND	Ground	76		GND	Ground

VI. Timing for Soft Control and Status Functions

Parameter	Symbol	Min.	Max.	Unit	Notes
MgmtInit Duration		-	2000	ms	
ResetL Assert Time	t_reset_init	10	-	μs	
IntL Assert Time	ton_IntL	-	200	ms	
IntL Deassert Time	toff_IntL	-	500	μs	
Rx LOS Assert Time	ton_losf	-	100	ms	
Flag Assert Time	ton_flag	-	200	ms	
Mask Assert Time	ton_mask	-	100	ms	
Mask Deassert Time	toff_mask	-	100	ms	
Module Select Wait Time	ModSelL Wait Time	-	N/A		Not support

VII. Timing for Squelch and Disable

Parameter	Symbol	Min.	Max.	Unit	Notes
Rx Squelch Assert Time	ton_Rxsq	-	50	ms	
Tx Squelch Assert Time	ton_Txsq	-	400	ms	
Tx Squelch Deassert Time	toff_Txsq	-	1500	ms	Based on modulation
Tx Disable Assert Time (fast mode)	ton_Txdisf	-	3	ms	
Tx Disable Deassert Time (fast mode)	toff_Txdisf	-	10	ms	
Rx Output Disable Assert Time	ton_Rxdis	-	100	ms	
Rx Output Disable Deassert Time	toff_Rxdis	-	100	ms	
Squelch Disable Assert Time	ton_sqdis	-	N/A	ms	Not support
Squelch Disable Deassert Time	toff_sqdis	-	N/A	ms	Not support

VIII. Digital Diagnostics

Parameter	Range	Accuracy	Unit	Calibration
Temperature	0 to 70	±3	ºC	Internal
Voltage	0 to Vcc	0.1	V	Internal
Tx Bias Current (Each Lane)	0 to 100	10%	mA	Internal
Tx Output Power (Each Lane)	-0.6 to +5.6	±3	dB	Internal
Rx Receive Power (Each Lane)	-18.6 to -4.4	±3	dB	Internal

IX. Diagram Mechanical Drawing