QSFP56 200GBASE-LR4 1310nm 10km Transceiver

QSFP56-LR4-200G-LL

Application

- Data Center 200GE 10km SMF links
- 5G backhaul
- Switch/Router interconnections

Features

- 200GBASE-LR4 compliant
  - 4x 26.5625 GBd PAM4
- 200GAUI-4 compliant
  - 4x 26.5625 GBd PAM4
- QSFP+ 28 Gb/s compliant
- LC connector
- <8.0W
- 0 to 70°C
- CMIS 4.0 management interface
- SFF-8636 management interface

FUNCTIONAL DESCRIPTION

Longline's TRQ5F20ENF is a fully integrated, 212.3 Gb/s optical transceiver for SMF links up to 10km. TRQ5F20ENF transmits data in compliance with the optical interface specification of IEEE 802.3bs, 200GBASE-LR4 and uses 4-level pulse amplitude modulation (PAM4) at 26.5625 Gbaud (GBd) operating at four wavelengths on a Local Area Network - wavelength division multiplexed (LAN-WDM) grid spaced at 5 nm from four cooled EA-DFB-LDs. The bit rate per lane is 53.125 Gb/s, which produces an aggregate data rate of 212.3 Gb/s by means WDM to the transmit port of the LC connector. The received optical lanes are de-multiplexed from the receive LC connector port to 4 PIN-PDs with low- power transimpedance amplifiers (TIAs) to recover the PAM4 for interfacing with the electrical interface.

The electrical interface is in compliance with 200GAUI-4 and specifies the use of four differential electrical lanes operating at 26.5625 GBd PAM4 per lane. The bit rate per lane is 53.125 Gb/s, resulting in an aggregate data rate of 212.3 Gb/s that matches the optical line interface.

The form factor of TRQ5F20ENF is compliant with the QSFP28 4X hardware specifications and management interface specifications (MIS) of the QSFP-DD multi-source agreement (MSA). QSFP56 modules can support up to four electrical lanes on the host interface, which is supported by QSFP28 or QSFP+ modules. The QSFP56 ports is that they are mechanically and electrically compatible with QSFP28 and QSFP+. Hence, the same port can be used to support multiple generations of modules and data rates if the networking hardware is designed for such operation. Its nose extends 15 mm beyond compact size defined by SFF-8661 Rev 2.5.
The SFF-8636 and CMIS 4.0 compliant 2-wire management interface enables control, alarm and monitoring of the TRQ5F20ENF.

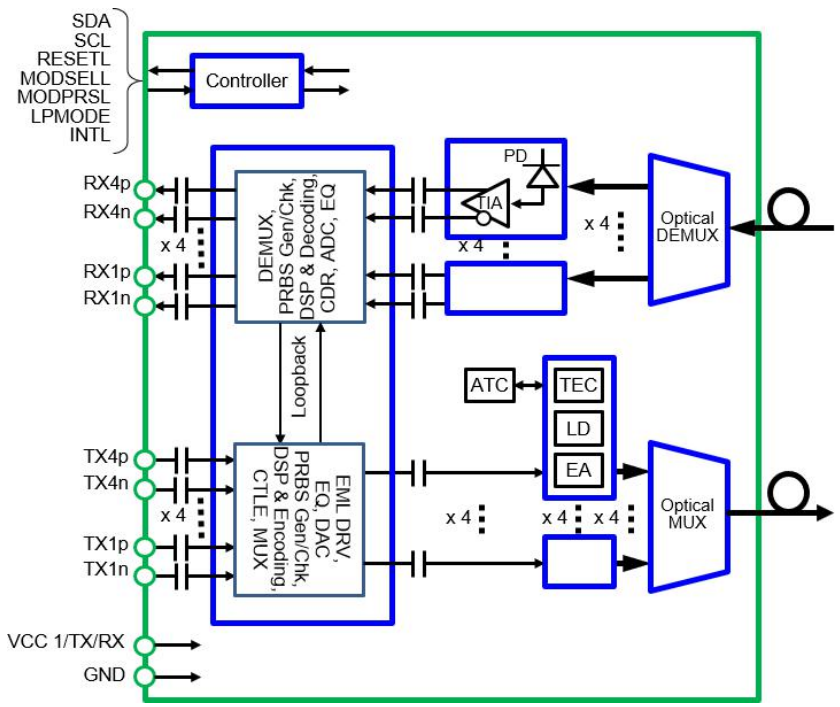

Figure 1 Functional Block Diagram

Description

Longline's TRQ5F20ENF-LF000, 200GBASE-LR4, hot pluggable optical transceiver is a high-performance solution for 200GE links for up to 10km over single mode fiber (SMF). It combines 4x 26.5625 GBd PAM4 electrical lanes into four 26.5625 GBd PAM4 optical channels in compliance with IEEE 200GBASE-LR4. Superior performance and reliability is achieved through FS's advanced transmitter and receiver design using cooled EA-DFB-LDs each at a LAN- WDM 1.3 µm wavelength and 4x PIN PDs with low-power TIAs. The 4 optical transmit and receive lanes are WDM'ed on to a single fiber pair through an LC connector.

Product Specifications

I. Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Remarks
Supply Voltage	Vcc	0	+3.6	V	+3.3V
Storage Temperature		-40	85	° C	
Optical Receiver Input		-	6.3	dBm	Average

II. Operating Environment

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply Voltage	Vcc	3.135	3.3	3.465	V	
Supply Voltage Noise Tolerance	PSNR	-	-	66	mV	10Hz–10MHz
Power Consumption		-	-	8.0	W	
Instantaneous peak current	Icc_ip_8			3200	mA	
Sustained peak current	Icc-sp_8			2640.2	mA	
Supply Current	Icc-8	--	-	2308.8	mA	Steadystate
Case Temperature	TC	0	25	70	° C	

III. Electrical Characteristics

Parameter	Min.	Typ.	Max.	Unit	Remarks
Transmitter					
Signaling rate per lane (range)	-100ppm	26.5625	+100ppn	GBd	
AC Common-mode output voltage (RMS)	-	-	17.5	mV	
Differential peak-to-peak output voltage	-	-	900	mV	
Near-end ESMW (Eye symmetry mask width)	0.265	-	-	UI	
Near-end Eye height, differential	70			mV	
Far-end ESMW (Eye symmetry mask width)	0.2	-	-	UI	
Far-end Eye height, differential	30	-	-	mV	
Far-end pre-cursor ISI ratio	-4.5	-	2.5	%	
Differential output return loss	Equation(83E-2)	-	-	dB	Note2
Common to differential mode conversion return loss	Equation(83E-3)	-	-	dB	Note2
Differential termination mismatch	-	-	10	%	
Transition time (20% to 80%)	9.5	-	-	ps	
DC common mode voltage	-350	-	2850	mV	
Receiver					
Signaling rate per lane (range)	-100ppm	26.5625	+100ppm	GBd	
Differential pk-pk input voltage tolerance	900	-	-	mV	atTP1a

Differential input return loss	Equation(83E-5)	-	-	dB	atTP1,Note2
Differential to common mode input return loss	Equation(83E-6)	-	-	dB	atTP1,Note2
Differential termination mismatch	-	-	10	%	atTP1
ESMW (Eye symmetry mask width)	0.22	-	-	UI	atTP1a
Eye width	0.22	-	-	UI	atTP1a
Applied pk-pk sinusoidal jitter	Table120E–6			MHz,UI	atTP1a
Eye height	32	-	-	mV	atTP1a
Single-ended input voltage tolerance range	-0.4	-	3.3	V	atTP1a
DC common mode voltage	-350	-	2850	mV	atTP1

Note:

1. Electrical module output is squelched for loss of optical input signal.
2. IEEE 802.3-2018 Section 6

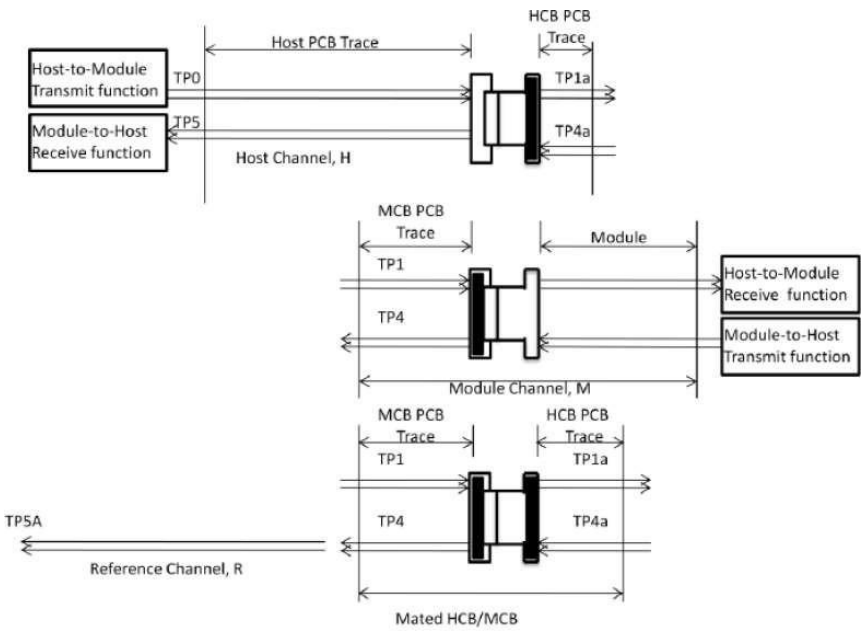

Figure 2 Reference Test Points

IV. Optical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
Channel data rate	fDC		53.125		Gbit/s	
Signaling rate, each lane	f_{SG}		26.5625		GBd	
Signal speed variation from nominal	Δf_{SG}	-100		+100	ppm	
Transmitter Center Wavelength						
Lane 0	Lane0	λ_{CT0}	1294.53		1296.59	
Lane 1	Lane1	λ_{CT1}	1299.02		1301.09	
Lane 2	Lane2	λ_{CT2}	1303.54		1305.63	
Lane 3	Lane3	λ_{CT3}	1308.09		1310.19	
Side-mode suppression ratio	SMSR	30			dB	
Total average launch power				11.3	dBm	
Average launch power, each lane		-3.4		5.3	dBm	Note1
Outer Optical Modulation Amplitude (OMAouter),each lane		-0.4		5.1	dBm	Note2
Difference in launch power between any two lanes(OMAouter)				4	dB	
Launch power in OMAouter minus TDECQ, each lane		-1.8-1.7			dBm	For ER≥4.5dB For ER<4.5dB
Transmitter and dispersion eye closure for PAM4, each lane	TDECQ			3.2	dB	
TDECQ –10log10(Ceq) (max)				3.2	dB	Note3

Average Optical Output Power of Off Transmitter	Poff			-30	dBm
Extinction Ratio	ER	3.5			dB
RIN15.6OMA				-132	dB/Hz
Optical return loss tolerance				15.6	dB
Transmitter reflectance				-26	dB
Average receive power, each lane		–9.7		5.3	dBm
Receive power (OMAouter), each lane				5.1	dBm
Difference in receive power between any two lanes (OMAouter)				4.2	dB
Receiver reflectance				-26	dB
Receiver sensitivity (OMAouter), each lanec		RS=max(-7.2,SECQ-8.6)			
Stressed receiver sensitivity (OMAouter), each lane				-5.4	dBm
Conditions of stressed receiver sensitivity test (Note 9)					
Stressed eye closure for PAM4 (SECQ), lane under test	SECQ	3.2	dB		
SECQ – 10log10(Ceq), lane under test				3.2	dB
OMAouter of each aggressor lane		-1.2	dBm		

Note:

1.Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.

2. Even if the TDECQ < 1.4 dB for an extinction ratio of ≥ 4.5 dB or TDECQ < 1.3 dB for an extinction ratio of < 4.5 dB, the OMAouter (min) must exceed this value.

3.Ceq is a coefficient defined in IEEE Std 802.3-2018 clause 121.8.5.3, which accounts for the reference equalizer noise enhancement.

4. Transmitter reflectance is defined looking into the transmitter.

5.Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.

6.For when Pre-FEC BER is 2.4 x 10^{-4}.

7.Receiver sensitivity (OMAouter), each lane (max) is informative and is defined for a transmitter with a value of SECQ up to 3.2 dB.

8.Measured with conformance test signal at TP3 (see IEEE Std 802.3-2018 clause 122.8.9) for the BER specified in IEEE Std 802.3-2018 clause 122.1.1.

9.These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

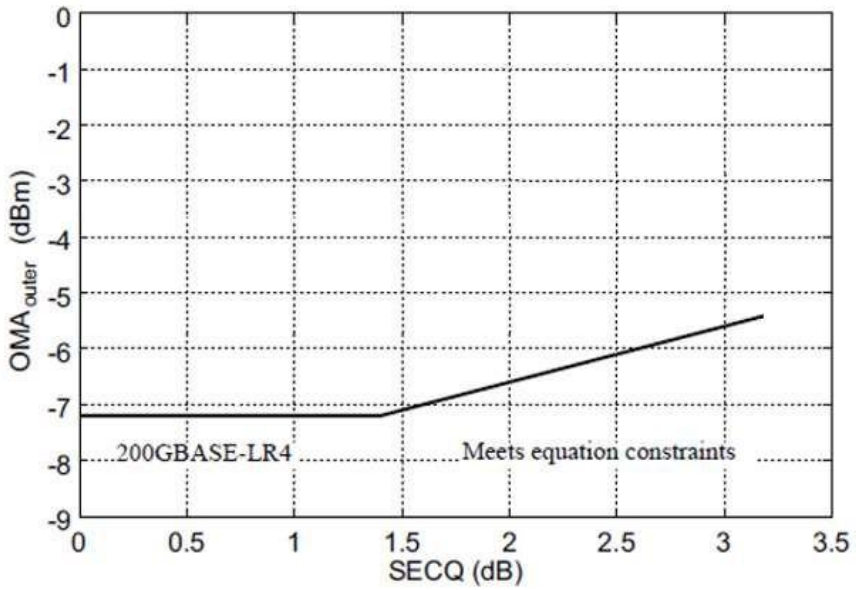

Figure 3 Receiver Sensitivity

V. RX_LOS Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
Receiver Loss of Signal Indicator Assert Level	RX_LOS	-30	-	-12.7	dBm	Averagepower
Receiver Loss of Signal Indicator De-assert Level	RX_LOS	-	-	-9.7	dBm	Averagepower

VI. HIGH SPEED DATA INTERFACE

Rx(n)(p/n)

Rx(n)(p/n) are module receiver data outputs. Rx(n)(p/n) are AC-coupled 100 Ohm differential lines that should be terminated with 100 Ohm differentially at the Host ASIC (SerDes). The AC coupling is inside the module and not required on the Host board. Output squelch for loss of optical input signal (Rx Squelch) shall function as follows: In the event of the optical signal on any channel becoming equal to or less than the level required to assert LOS, then the receiver data output for that channel shall be squelched or disabled. In the squelched or disabled state output impedance levels are maintained while the differential voltage swing shall be less than 50 mVpp.

Tx(n)(p/n)

Tx(n)(p/n) are module transmitter data inputs. They are AC-coupled 100 Ohm differential lines with 100 Ohm differential terminations inside the module. The AC coupling is inside the module and not required on the Host board.
Output squelch (Tx Squelch) for loss of input signal (Tx LOS) is supported. In the event of the differential, peak-to-peak electrical signal on any channel becomes less than 50 mVpp, then the transmitter optical output for that channel shall be squelched and the associated TxLOS flag set. Where squelched, the transmitter OMA shall be less than or equal to -26 dBm.

VII. CONTROL INTERFACE

Low Speed Control Pins

In addition to the 2-wire serial interface the transceiver has the following low speed signals for control and status: ModSelL, ResetL, InitMode, ModPrsL and IntL. See the QSFP28 Electrical Specification for detailed descriptions of each signal.

Low Speed Electrical Specifications

Low speed signaling other than SCL and SDA is based on Low Voltage TTL (LVTTL) operating at Vcc.

Low Speed Control and Sense Signals

Parameter	Symbol	Min	Max	Unit	Condition
SCL and SDA	VOL	0	0.4	V	IOL(max)=3.0mA
	VOH	Vcc-0.5	Vcc+0.3	V	
SCL and SDA	VIL	-0.3	Vcc*0.3	V	
	VIH	VCC*0.7	Vcc+0.5	V	
Capacitance for SCL and SDA I/O pin	Ci		14	pF	
Total bus capacitive load for SCL and SDA	Cb		100	pF	3.0 k Ohms pull-up resistor max
			200	pF	1.6 k Ohms pull-up resistor max
LPMode, Reset and ModSelL	VIL	-0.3	0.8	V	
	VIH	2	VCC+0.3	V	
	Iin	-365	125	uA	0 V ≤ Vin ≤ Vcc
ModPrsL and IntL	VOL	0	0.4	V	IOL=2.0mA
	VOH	VCC-0.5	VCC+0.3	V	

2-Wire Management Interface

A management interface, as already commonly used in other form factors like QSFP, SFP, and CDFP, is specified in order to enable flexible use of the module by the user. This QSFP56 specification is based on SFF-8636 [7] but with modifications to support the QSFP-DD Management Interface Specification [6], and as such is not directly backwards compatible with SFF-8636 [7]. Byte 00 on the Lower Page or Address 128 Page 00 is used to indicate the use of the QSFP-DD memory map rather than the QSFP memory map.

The QSFP56 Module supports alarm, control and monitor functions via a two-wire interface bus. Upon module initialization, these functions are available. QSFP56 two-wire electrical interface consists of 2 pins of SCL (2-wire serial interface clock) and SDA (2-wire serial interface data). The low speed signaling is based on Low Voltage CMOS (LVCMOS) operating at Vcc. Hosts shall use a pull-up resistor connected to Vcc_host on the 2-wire interface SCL (clock) and SDA (Data) signals. The timing requirements on the two-wire interface are listed in Table 7 and Figure 4.

Management Interface Timing

Parameter	Symbol	Min	Max	Unit	Conditions
Clock Frequency	fSCL	0	1000	kHz	
Clock Pulse Width Low	tLOW	0.50		µs	
Clock Pulse Width High	tHIGH	0.26		µs	
Time bus free before new transmission can start	tBUF	1		µs	Between STOP and START and between ACK and ReStart
START Hold Time	tHD.STA	0.26		µs	The delay required between SDA becoming low and SCL starting to go low in a START
START Setup Time	tSU.STA	0.26		µs	The delay required between SCL becoming high and SDA starting to go low in a START
Data In Hold Time	tHD.DAT	0		µs	
Data In Setup Time	tSU.DAT	0.1		µs	
Input Rise Time	tR		120	ns	From(VIL,MAX=0.3*Vcc)to(VIH,MIN=0.7*Vcc)
Input Fall Time	tF		120	ns	From(VIH,MIN=0.7*Vcc)to(VIL,MAX=0.3*Vcc)
STOP Setup Time	tSU.STO	0.26		µs	
STOP Hold Time	tHD.STO	0.26		us	
Aborted sequence bus release	Deselect_Abort		2	ms	Delay from a host de-asserting ModSelL (at any point in a bussequence) to the QSFP-DD module releasing SCL and SDA

ModSelL Setup Time[1]	tSU.ModSelL	2		ms	ModSelL Setup Time is the setuptime on the select lines before the start of a host initiated serial bussequence.
ModSelL Hold Time[1]	tHD.ModSelL	2		ms	ModSelL Hold Time is the delayfrom completion of a serial bussequencetochangesofmoduleSelectstatus.
Serial Interface Clock Holdoff "Clock Stretching"	T_clock_hold		500	us	Maximum time the QSFP-DD module may hold the SCL line low before continuing with a read or write operation
Complete Single or Sequential Write to nonvolatile registers	tWR		80	ms	Complete Write of up to 8 Bytes
Accept a single or sequential write to volatile memory	tNACK		80	ms	Time required for the module to accept a single or sequential write to volatile memory.
Endurance (Write Cycles)		50k			Module Case Temperature=70° C

Note:

1. When the host has determined that module is QSFP56, the management registers can be read to determine alternate supported ModSelL set up and hold times.

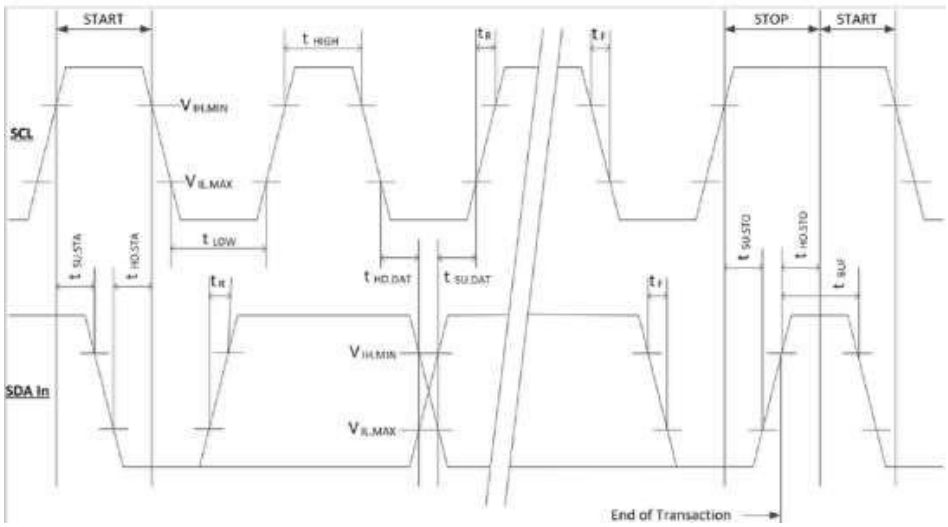

Figure 4 2-Wire Interface Timing Diagram

Control and Status Timing Requirements

Parameter	Symbol	Min	Max	Unit	Conditions
MgmtInitDuration	Max MgmtInit Duration		2000	ms	Time from power on[1],hot plug or rising edge of reset until completion of the MgmtInit State
ResetL Assert Time	t_reset_init	10		µs	Minimum pulse time on the ResetL signal to initiate a module reset.
IntL Assert Time	ton_IntL		200	ms	Time from occurrence of condition triggering IntL until Vout:IntL=Vol
IntL De-assert Time	toff_IntL		500	µs	Time from clear on read[2] operation of associated flag until Vout:IntL=Voh. This includes deassert times for Rx LOS,Tx Fault and other flagbits.
Rx LOS Assert Time	ton_los		100	ms	Time from Rx LOS condition present to Rx LOS bit set (value=1b) and IntL asserted.
Rx LOS Assert Time (optional fast mode)	ton_losf		100	ms	Time from Rx LOS state to Rx LOS bit set (value=1b) and IntL asserted.
Rx LOS De-assert Time (optional fast mode)	toff_losf		100	ms	Time from Rx LOS condition absent to negation of Rx LOS statusbit.
Tx Fault Assert Time	ton_Txfault		200	ms	Time from Tx Fault state toTx Fault bit set (value=1b) and IntL asserted.
Flag Assert Time	ton_flag		200	ms	Time from occurrence of condition triggering flag to associated flag bit set (value=1b) and IntL asserted.
Mask Assert Time	ton_mask		100	ms	Time from mask bit set (value=1b) [3]until associated IntL assertion is inhibited
Mask De-assert Time	toff_mask		100	ms	Time from mask bit cleared (value=0b)[3] until associated IntL operation resumes
Application or Rate Select Change Time	t_ratesel		100	ms	Time from change of state of Application or Rate Select bit[3] until transmitter or receiver bandwidth is in conformance with appropriate specification

Note:

1. Power on is defined as the instant when supply voltages reach and remain at or above the minimum level specified in Table 7.
2. Measured from the rising edge of SDA in the stop bit of the read transaction.
3. Measured from the rising edge of SDA in the stop bit of the write transaction.
4. Rx LOS condition is defined at the optical input by the relevant standard.

Squelch & TxRx Disable Timing

Parameter	Symbol	Max	Unit	Conditions
Rx Squelch Assert Time	ton_Rxsq	15	ms	Time from loss of Rx input signal until the squelched output condition is reached.
Rx Squelch De-assert Time	toff_Rxsq	(5000)	ms	Time from resumption of Rx input signals until normal Rx output condition is reached.
Tx Squelch Assert Time	ton_Txsq	400	ms	Time from loss of Tx input signal until the squelched output condition is reached.
Tx Squelch De-assert Time	toff_Txsq	(5000)	ms	Time from resumption of Tx input signals until normal Tx output condition is reached.
Tx Disable Assert Time	ton_txdis	100	ms	Time from the stop condition of the Tx Disable write sequence[1] until optical output falls below 10% of nominal
Tx Disable Assert Time (optional fast mode)	ton_txdisf	3	ms	Time from Tx Disable bit set (value=1b)[1] until optical output falls below 10% of nominal
Tx Disable De- assert Time	toff_txdis	400	ms	Time from Tx Disable bit cleared (value=0b)[1] until optical output rises above 90% of nominal
Tx Disable De- assert Time (optional fast mode)	toff_txdisf	10	ms	Time from Tx Disable bit cleared (value =0b)[1] until optical output rises above 90% of nominal
Rx Output Disable Assert Time	ton_rxdis	100	ms	Time from Rx Output Disable bit set (value=1b)[1] until Rx output falls below10% of nominal
Rx Output Disable De- assert Time	toff_rxdis	100	ms	Time from Rx Output Disable bit cleared (value=0b)[1] until Rx output rises above 90% of nominal
Squelch Disable Assert Time	ton_sqdis	Not applicable (Tx/Rx Auto Squelch Disable not supported)		This applies to Rx and Tx Squelch and is the time from bit set (value=0b)[1] until squelch functionality is disabled.
Squelch Disable De-assert Time	toff_sqdis	Not applicable (Tx/Rx Auto Squelch Disable not supported)		This applies to Rx and Tx Squelch and is the time from bit cleared (value=0b)[1] until squelch functionality is enabled

Note:

1. Measured from LOW to HIGH SDA signal transition of the STOP condition of the write transaction.

VIII. POWER

The circuit card in a QSFP56 module has three designated power pins, labeled VccTx, VccRx and Vcc1. When the QSFP56 module is "hot plugged" into a connector with power already present, the three pins have power applied concurrently. The module is responsible for limiting the inrush current surge during a hot plug event. The host power supply is responsible for supplying up to the maximum inrush current limits during a hot plug event without causing disturbance to other modules and components on the same power supply.

QSFP56 modules are categorized into several power classes as listed in Table 10. The power class of TRQ5F20 is class 8.

Power Class	Maximum power consumption per module (W)
1	1.5
2	2.0
3	2.5
4	3.5
5	4.0
6	4.5
7	5.0
8	10.0 (Note)

Note: For power class 8, maximum power consumption is declared by the module in SFF-8636 [7], Page 00h, Byte 107.

Host Board Power Supply Filtering

The host board should use the power supply filtering equivalent to that shown in Figure 5.

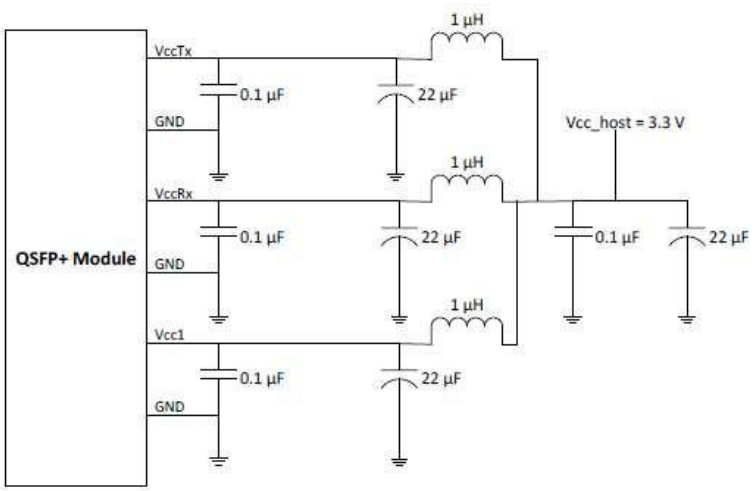

Figure 5 Recommended Host Board Power Supply Filtering

Module Power Supply Specification

In order to avoid exceeding the host system power capacity, upon hot-plug, power cycle or reset, all QSFP56 modules shall power up in Low Power Mode if LPMode is asserted. If LPMode is not asserted, the module will proceed to High Power Mode without host intervention. Figure 6 shows waveforms for maximum instantaneous, sustained and steady state currents for Low Power and High Power modes. Specification values for maximum instantaneous, sustained and steady state currents at each power class are given in Table 2.

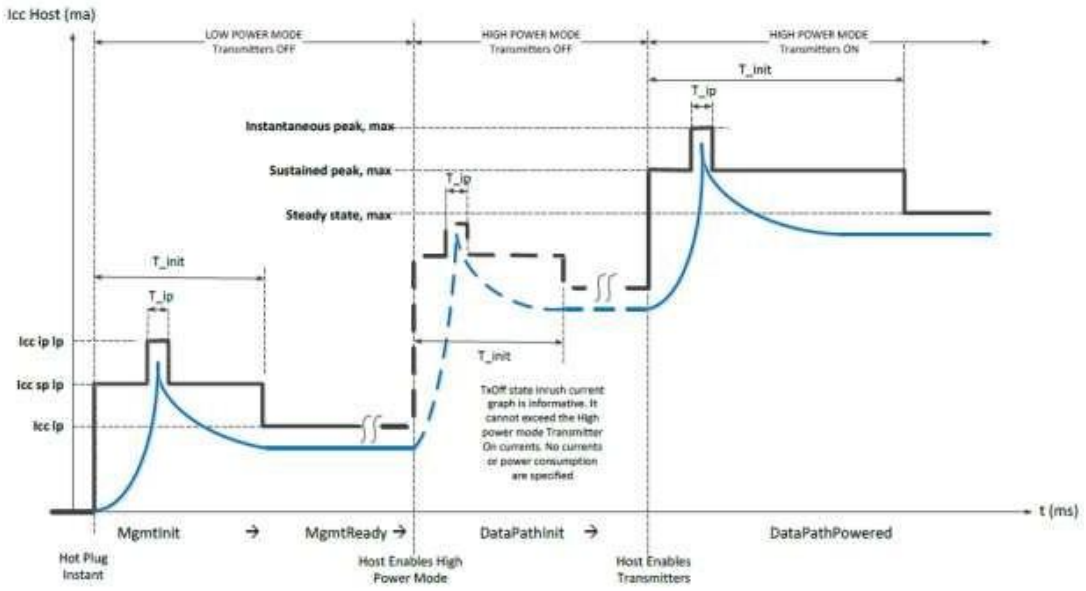

Figure 6 Instantaneous and Sustained Peak Currents for Icc Host

IX. Pin Assignment and Desription

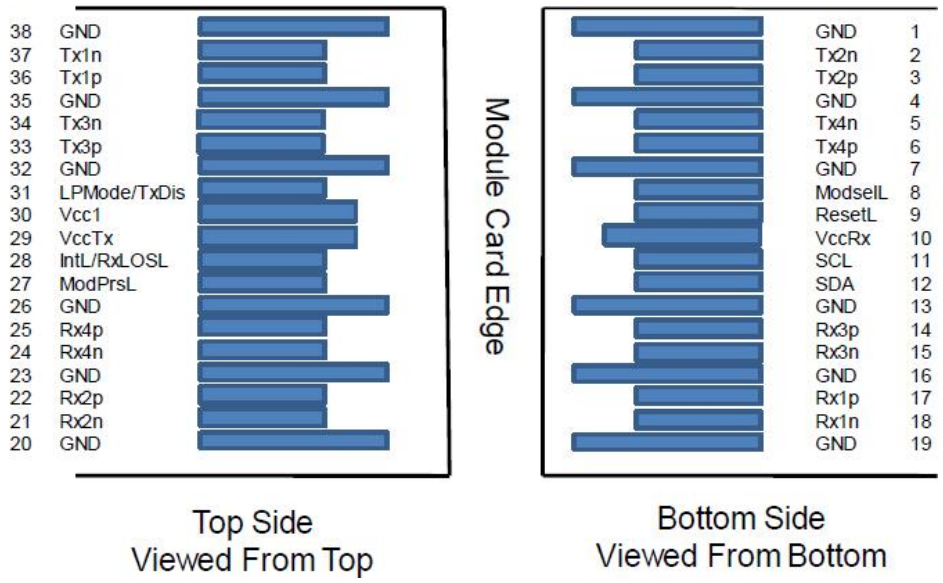

Figure 7 Module Pad Layout

Pin Description

Pad	Logic	Symbol	Description	Plug Seq-uence	Note
1		GND	Ground	1	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3	
4		GND	Ground	1	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3	
7		GND	Ground	1	1
8	LVTTL-I	ModSelL	Module Select	3	
9	LVTTL-I	ResetL	Module Reset	3	
10		VccRx	+3.3V Power Supply Receiver	2	2
11	LVCMOS-I/O	SCL	Two-wire interface clock	3	
12	LVCMOS-I/O	SDA	Two-wire interface data	3	
13		GND	Ground	1	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3	
15	CML-O	Rx3n	Receiver Inverted Data Output	3	
16		GND	Ground	1	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3	
18	CML-O	Rx1n	Receiver Inverted Data Output	3	
19		GND	Ground	1	1
20		GND	Ground	1	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3	
23		GND	Ground	1	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3	
26		GND	Ground	1	1
27	LVTTL-O	ModPrsL	Module Present	3	
28	LVTTL-O	IntL/RxLOSL	Interrupt. Optionally configurable as RxLOSL via the management interface (SFF-8636).	3	
29		VccTx	+3.3V Power supply transmitter	2	2
30		Vcc1	+3.3V Power supply	2	2
31	LVTTL-I	LPMode/TxDis	Low Power Mode. Optionally configurable as TxDis via the management interface (SFF-8636).	3	
32		GND	Ground	1	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3	
35		GND	Ground	1	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3	
38		GND	Ground	1	1
Note 1: GND is the symbol for signal and supply (power) common for the module. All are common within the module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.					
Note 2: VccRx, Vcc1 and VccTx are applied concurrently and may be internally connected within the module in any combination. Vcc contacts in SFF-8662 and SFF-8672 each have a steady state current rating of 1 A.					

X. MECHANICAL DIMENSIONS

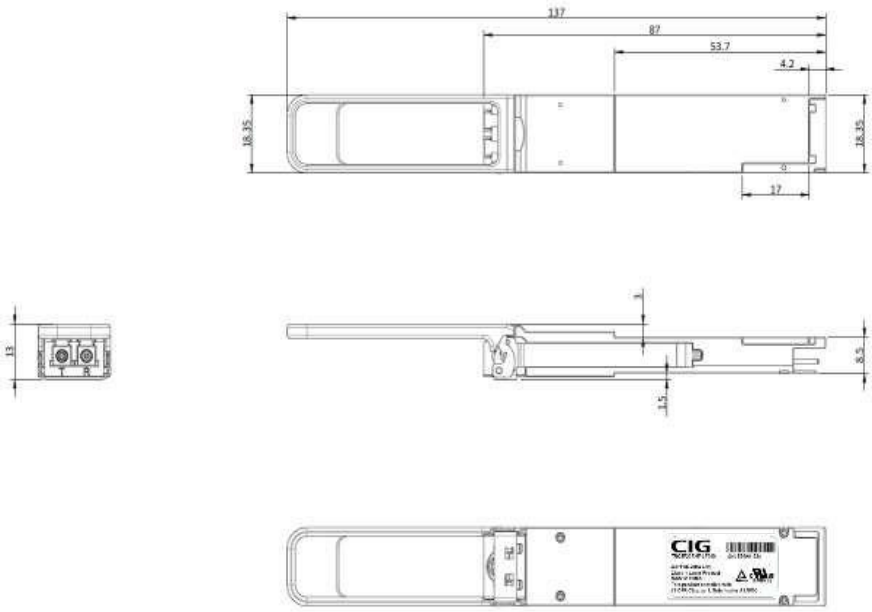

Figure 8 Mechanical Dimensions

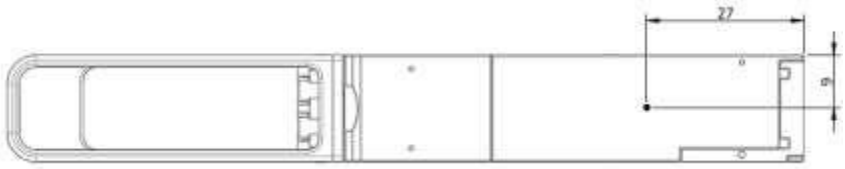

Figure 9 Case temperature measurement point