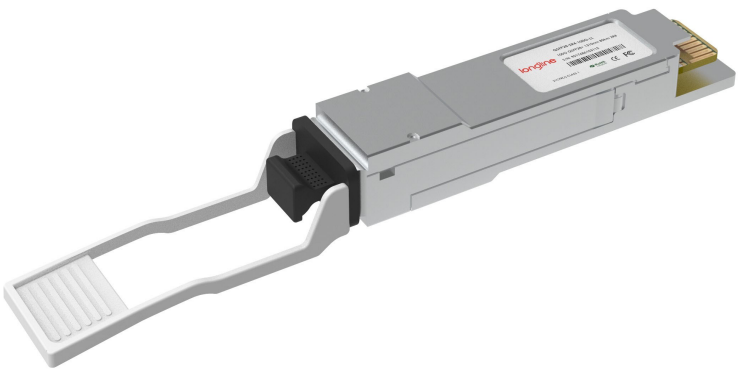
100GBASE-ZR4 QSFP28 1310nm 80km DOM Optical Transceiver Module

QSFP28-ZR4-100G-LL



Application

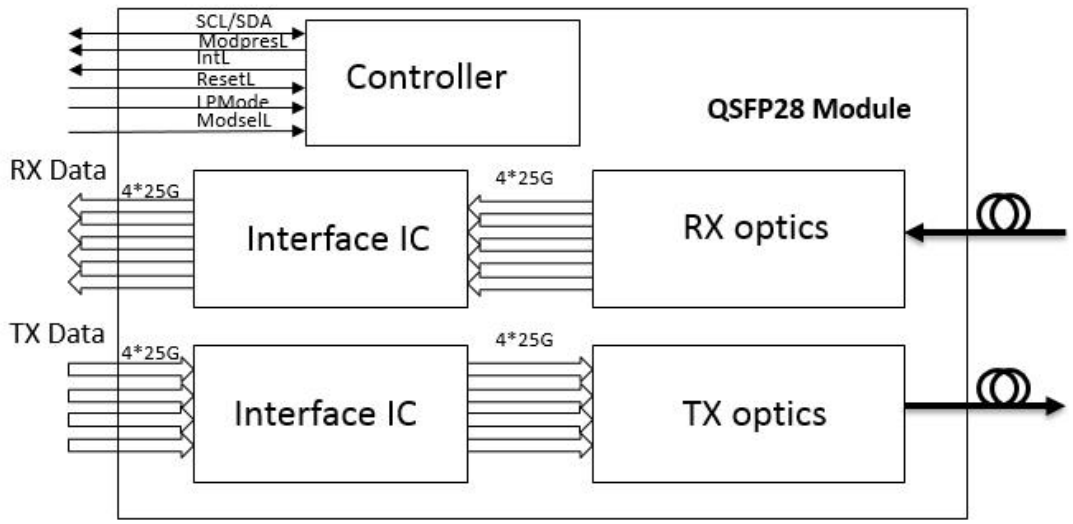
- 100GBASE-ZR4 100G Ethernet
- Telecom Networking

Features

- QSFP28 MSA compliant
- Compliant to 4-Wavelength WDM MSA
- Digital diagnostic monitoring support
- Hot pluggable 38 pin electrical interface
- 4 LAN-WDM lanes MUX/DEMUX design
- 4x25G electrical interface
- Supports 103.125Gb/s aggregate bit rate
- Up to 80km transmission on single mode fiber
- LC duplex connector
- Single 3.3V power supply
- RoHS-6 compliant
- Operating case temperature: 0℃ to 70℃

Description

Longline's QSFP28-ZR4-100G is designed for 80km optical communication applications. This module contains 4-lane optical transmitter, 4-lane optical receiver and module management block including 2 wire serial interface. The optical signals are multiplexed to a single-mode fiber through an industry standard LC connector. A block diagram is shown as follows.



ModSelL:
The ModSelL is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple modules on a single 2-wire interface bus. When the ModSelL is "High", the module shall not respond to or acknowledge any 2-wire interface communication from the host. ModSelL signal input node shall be biased to the "High" state in the module.
In order to avoid conflicts, the host system shall not attempt 2-wire interface communications within the ModSelL de-assert time after any modules are deselected. Similarly, the host shall wait at least for the period of the ModSelL assert time before communicating with the newly selected module. The assertion and de-asserting periods of different modules may overlap as long as the above timing requirements are met.

ResetL :
The ResetL pin shall be pulled to Vcc in the module. A low level on the ResetL pin for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t_init) starts on the rising edge after the low level on the ResetL pin is released. During the execution of a reset (t_init) the host shall disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by asserting "low" an IntL signal with the Data_Not_Ready bit negated. Note that on power up (including hot insertion) the module should post this completion of reset interrupt without requiring a reset.

LPMode:
The LPMode pin shall be pulled up to Vcc in the module. The pin is a hardware control used to put modules into a low power mode when high. By using the LPMode pin and a combination of the Power override, Power_set and High_Power_Class_Enable software control bits (Address A0h, byte 93 bits 0,1,2).

ModPrsL:
ModPrsL is pulled up to Vcc_Host on the host board and grounded in the module. The Mod- PrsL is asserted "Low" when inserted and de-asserted "High" when the module is physically absent from the host connector.

IntL:
IntL is an output pin. When IntL is "Low", it indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL pin is an open collector output and shall be pulled to host supply voltage on the host board. The INTL pin is de-asserted "High" after completion of reset, when byte 2 bit 0 (Data Not Ready) is read with a value of '0' and the flag field is read (see SFF-8636).

Product Specifications

I. Absolute Maximum Ratings

It has to be noted that the operation in of any individual absolute maximum ratings might cause permanent damage to this module.

Parameter	Symbol	Min	Typ.	Max	Unit	Ref.
Maximum Supply Voltage	Vcc	-0.3	3.3	3.6	V	
Storage Temperature	Ts	-40		85	℃	
Relative Humidity	RH	15		85	%	1
Damage Threshold, four lanes on	THd	5.5			dBm	

Notes:

1.Non-condensing

II. Recommended Operating Environment

Electrical and optical characteristics below are defined under this operating environment, un- less otherwise specified.

Parameter	Symbol	Min	Typ.	Max	Unit	Ref.
Supply Voltage	Vcc	3.135	3.3	3.465	V	
Case Temperature	Top	0		70	℃	
Link Distance with G.652				80	km	

III. Electrical Characteristics

Parameter	Symbol	Min	Typ.	Max	Unit	Ref.
Power dissipation				6	W	
Supply Current	Icc			1.7316	A	Steady state

Transmitter

Data Rate, each lane			25.78125		Gbps	
Differential Voltage pk-pk	Vpp			900	mV	At 1 MHz
Common Mode Voltage	Vcm	-350		2850	mV	
Transition time	Trise/Tfall	10			ps	20%~80%
Differential Termination Resistance Mismatch				10	%	
Eye width	EW15	0.46			UI	
Eye height	EH15	95			mV	

Receiver

Data Rate, each lane			25.78125		Gbps	
Differential Termination Resistance Mismatch				10	%	At 1 MHz
Differential output voltage	Vout, pp	100		400	mV	1
		300		600		
		400		800		
		600		1200		
Common Mode Noise, RMS	Vrms			17.5	mV	
Transition time	Trise/Tfall	12			ps	20%~80%
Eye width	EW15	0.57			UI	
Eye height	EH15	228			mV	

Notes:

1.Output voltage is settable in 4 discrete ranges via I2C. Default range is 400 – 800 mV.

IV. Optical Characteristics

100GBASE-ZR4 Operation（EOL, TOP ＝0 to +70 C, VCC＝3.135 to 3.465 Volts）

Parameter	Min	Typ.	Max	Unit	Ref.
Transmitter					
Signaling Speed per Lane		25.78125 ± 100 ppm		Gb/s	
Receive wavelengths	1294.53		1296.59	nm	
	1299.02		1301.09		
	1303.54		1305.63		
	1308.09		1310.19		
Side-Mode Suppression Ratio (SMSR)	30			dB	
Total Average Launch Power	8		12.5	dBm	
Average launch power, each lane	2		6.5	dBm	
Optical Modulation Amplitude (OMA), each lane				dBm	
Difference in launch power between any two lanes (Average and OMA)			3	dBm	
Transmitter and Dispersion Penalty (TDP), each lane			TBD	dB	
Average launch power of OFF transmitter, each lane (max)			-30	dBm	
Extinction Ratio (ER)	6			dB	
RIN OMA			-130	dB/Hz	
Optical return loss tolerance (Max)			20	dB	
Transmitter reflectance			-12	dB	
Transmitter eye mask definition {X1, X2, X3, Y1, Y2, Y3}		{0.25, 0.4, 0.45, 0.25, 0.28, 0.4}			1
Mask margin	5			%	

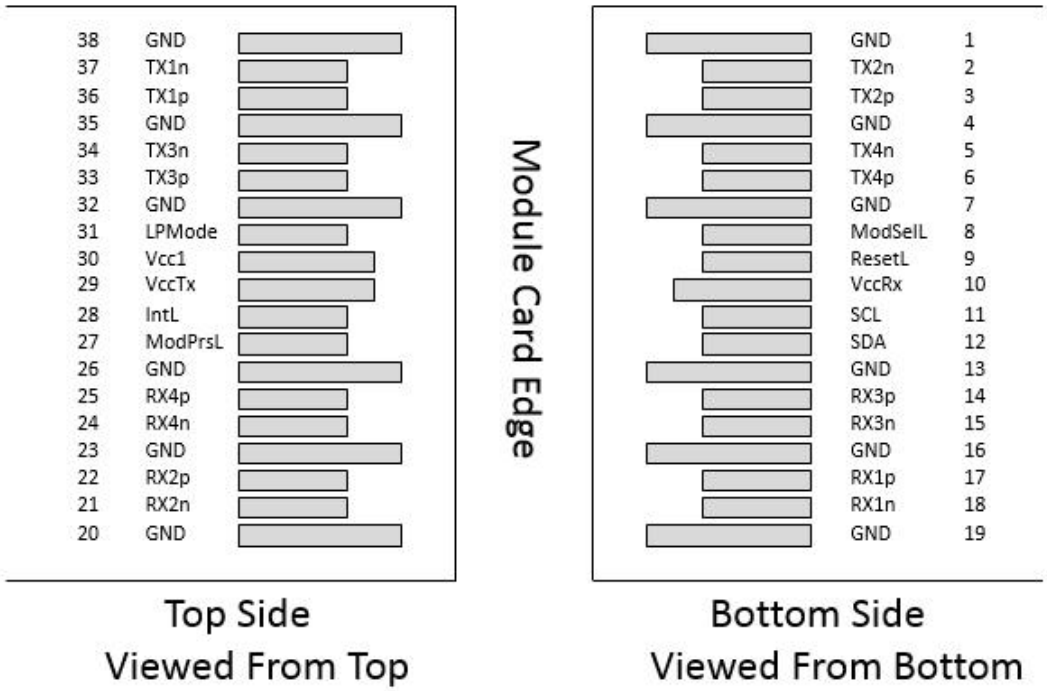
Receiver

Signaling Speed per Lane		25.78125 ± 100 ppm		Gb/s	
Receive wavelengths	1294.53		1296.59	nm	
	1299.02		1301.09		
	1303.54		1305.63		
	1308.09		1310.19		
Average receiver power, each lane	-28		2	dBm	
Receiver power, each lane (OMA)				dBm	
Receiver reflectance			-26		
Receiver sensitivity (OMA), each lane			<-28	dBm	
Receiver sensitivity Average, each lane			TBD	dBm	1
Stressed receiver Sensitivity (OMA) , each lane				dBm	
Receiver 3 dB electrical upper cutoff frequency, each lane			31		
Damage threshold, each lane	-6			dBm	
Saturation Power（EOL）	-7			dBm	
LOS Assert	-40			dBm	
LOS Deassert			-31	dBm	
LOS Hysteresis	0.5			dB	

Notes:

1.Measured with 25.78125 Gb/s, PRBS-31 NRZ, ER>6dB (ZR4), BER<5E-5

V. Pin Assignment



Pin	Symbol	Description	Notes
1	GND	Ground	1
2	Tx2n	Transmitter Inverted Data Input	
3	Tx2p	Transmitter Non-Inverted Data Input	
4	GND	Ground	1
5	Tx4n	Transmitter Inverted Data Input	
6	Tx4p	Transmitter Non-Inverted Data Input	
7	GND	Ground	1
8	ModSelL	Module Select	
9	ResetL	Module Reset	
10	VccRx	+3.3 V Power Supply Receiver	
11	SCL	2-wire serial interface clock	
12	SDA	2-wire serial interface data	
13	GND	Ground	1

14	Rx3p	Receiver Non-Inverted Data Output	
15	Rx3n	Receiver Inverted Data Output	
16	GND	Ground	1
17	Rx1p	Receiver Non-Inverted Data Output	
18	Rx1n	Receiver Inverted Data Output	
19	GND	Ground	1
20	GND	Ground	1
21	Rx2n	Receiver Inverted Data Output	
22	Rx2p	Receiver Non-Inverted Data Output	
23	GND	Ground	1
24	Rx4n	Receiver Non-Inverted Data Output	
25	Rx4p	Receiver Inverted Data Output	
26	GND	Ground	1
27	ModPrsL	Module Present	
28	IntL	Interrupt	
29	VccTx	+3.3V Power supply transmitter	
30	Vcc1	+3.3V Power supply	
31	LPMode	Low Power Mode	
32	GND	Ground	1
33	Tx3p	Transmitter Non-Inverted Data Input	
34	Tx3n	Transmitter Inverted Data Input	
35	GND	Ground	1
36	Tx1p	Transmitter Non-Inverted Data Input	

37	Tx1n	Transmitter Inverted Data Input	
38	GND	Ground	1

Notes:

1.Circuit ground is internally isolated from chassis ground.

VI. Diagram Mechanical Drawing