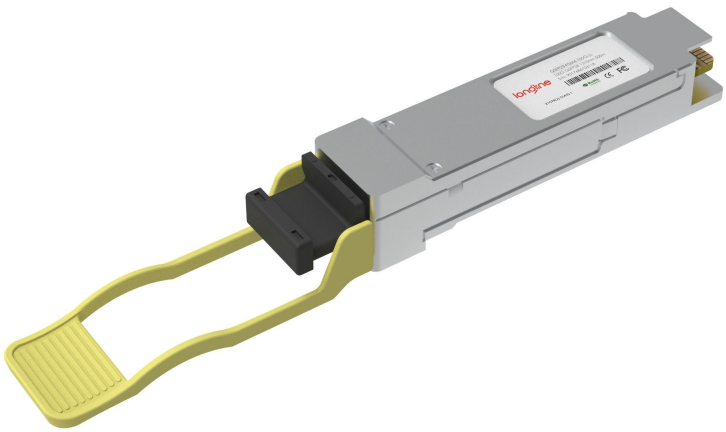
100GBASE-PSM4 QSFP28 1310nm 2km Transceiver

QSFP28-PSM4-100G-LL



Application

- Data Center 100GE 2km Parallel Links
- Enterprise LAN

Features

- MPO-12 Optical Connector
- Tx Input Equalizer
- 100G PSM4 MSA Compliant
- 4x25G PIN Receiver
- Built-in Digital Diagnostic Functions
- 4x25G 1310nm Uncooled DFB Transmitter
- Single +3.5V Power Supply
- Operating Temperature Range: 0℃ to 70℃
- SFF-8636 Management Interface

Description

The 100G PSM4 QSFP28, hot pluggable optical transceiver interfacing to a CAUI-4 electrical interface and providing 4 lanes of NRZ 25 Gb/s over 4 single mode fiber (SMF) pairs up to a distance of 2km via a 12-fiber MPO connector. This simple architecture enables a cost-effective 100GE switch/router port density .

Functional Description

The PSM4 QSFP28 optical transceiver is a monolithic electronic and photonic module assembly containing four 1310nm optical lanes each operating at data rates up to 25 Gb/s. The optical interface of the module is a 12-fiber MPO receptacle compliant to 100G PSM4 MSA.

It provides an excellent solution for 100G applications where cost-effective high port density is needed.

The device is in the QSFP28 form factor with digital diagnostics monitoring functionalities (DDM) and control functions. DDM functionality (alarm and warning features) is integrated into the design via an I2C serial interface per the Multi-Source Agreement (MSA) SFF8636, Rev. 2.5.

Product Specifications

I. Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only.

Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet.

Exposure to absolute maximum ratings will cause permanent damage and/or adversely affect device reliability.

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Storage Temperature Range	T_{ST}	-40	-	85	℃	1, 2
Operating Case Temperature	T_{OP}	0	-	70	℃	1, 2
Operating Relative Humidity	RH	15	-	85	%	1, 2, 3
Supply Voltage Range	V_{CC}	0	-	3.6	V	1, 2
Supply Voltage Range	V_{CC}	-0.5	-	V_{CC}+0.3	V	1, 2

Notes:

1. Absolute Maximum Ratings are those beyond which damage to the device may occur.
2. Between the Recommended Operating conditions and Absolute Maximum ratings, prolonged operation is not intended, and permanent device degradation may occur.
3. Non-condensing.

II. Operating Conditions

Electrical and optical characteristics below are defined under this operating environment, unless otherwise specified.

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Data Rate	DR		103.1		Gb/s	
Operating Case Temperature	T_{OP}	0		70	℃	
Bit Error Rate	BER			5E-5		
Fiber Length on SMF per G.652	L			2000	m	1
Loss budget over SMF per G.652				5	dB	2
Supply Voltage	Vcc	3.135		3.465	V	
Module Power – Normal mode	P			3.5	W	
Module Power – Low power mode	P			1.5	W	

Notes:

1. Tested with PRBS31, 5dB loss budget with FEC on the host.
2. The channel insertion loss budget may include up to 1dB MPI loss penalty with worst case transmitter and worst case connector MPI.

III. Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Transmitter						

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Transmitter						
Differential Input Impedance	Z_d		100		Ω	
Differential Input Voltage				900	mV	
Differential Termination Mismatch			10		%	
Differential Input Return Loss@ 0.01–8 GHz	SDD11	9.5-0.37f			dB	1
Differential Input Return Loss@ 8 – 19 GHz		4.75-7.4log10 (f/14)			dB	1
Differential to Common Mode Output Return Loss@0.01-12.89GHz	SCD11	22-20(f/25. 78)			dB	1
Differential to Common Mode Output Return Loss@12.89 – 19 GHz		15 -6(f/25.7 8)			dB	1
BER with stressed input signal				$1x10^{-15}$		2
DC common mode voltage		-350		2850	mV	
Receiver						
Differential Output impedance	Z_d		100		Q	
Differential Output Voltage				900	mV	
DC common mode voltage		-350		2850	mV	
AC common-mode output voltage				17.5	mV	
Vertical eye closure	VEC			5.5	dB	
Eye width		0.57			UI	
Eye height, differential		228			mV	
Rx Output Data Total Jitter				0.43	UI	
Transition Time (min, 20% to 80%)	t_{RH},t_{FH}	12			Ps	

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Receiver						
Differential Output Return Loss@ 0.01–8GHz	SDD22	9.5-0.37f			dB	1
Differential Output Return Loss@ 0.01–8GHz		4.75-7.4log1 0(f/14)			dB	1
Common Mode to Differential Output Returnloss@ 0.01 -12.89 GHz	SDC22	22-20(f/25. 78)			dB	1
Common Mode to Differential Output Returnloss@12.89 – 25.78 GHz		15 -6(f/25.7 8)			dB	1

Notes:

1. f is frequency in GHz

2. per IEEE802.3bm Annex 83E.3.4.1

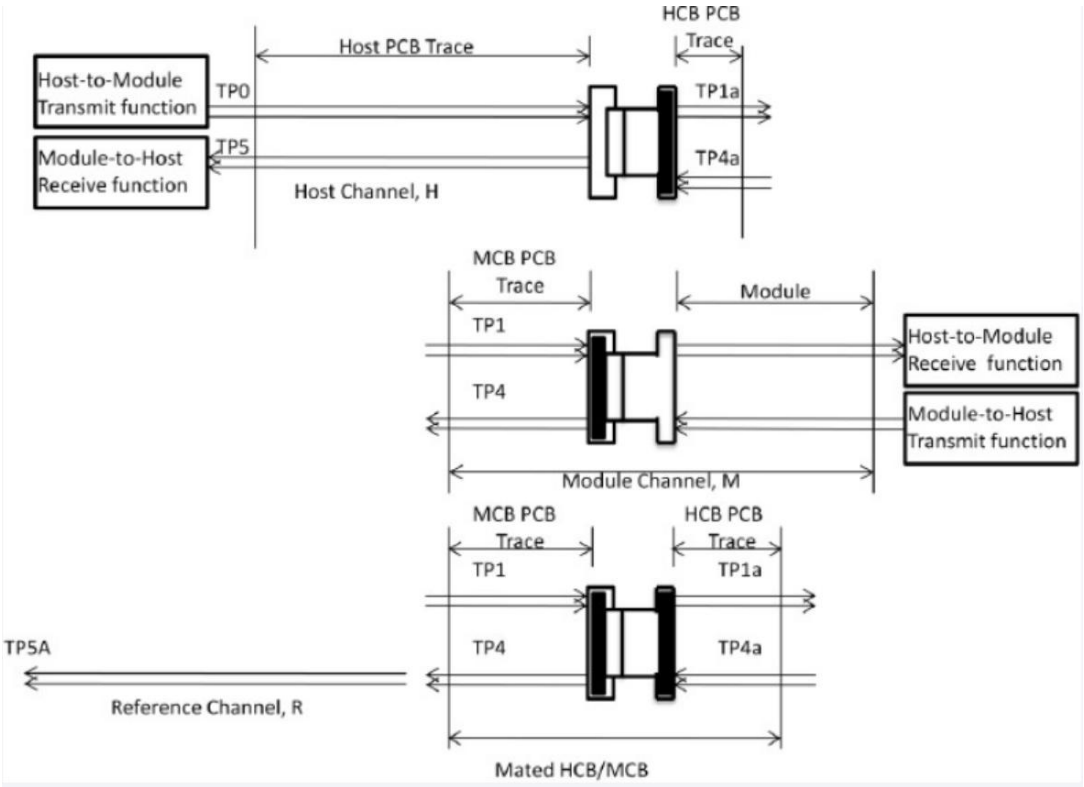


Figure 1 Reference Test Points

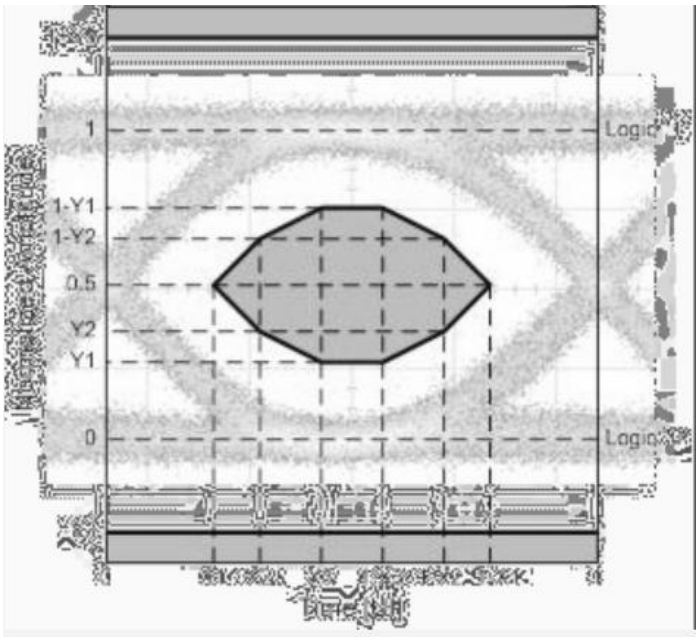
IV. Optical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Transmitter						
Signaling Speed (±100ppm, Per Lane)	B		25.78125		Gb/s	
Center Wavelength	λ	1295	1310	1325	nm	
Total Average Launch Power(All Lane)				+8	dBm	
Average Launch Power, each Lane	Pavg	-9.4		2	dBm	1
Difference in Launch Power Between any Two Lanes (OMA)				5	dB	
Optical Modulation Amplitude (per Lane)	POMA	-4		2.2	dBm	
Tx_OMA-TDP		-5			dBm	
Extinction Ratio	ER	3.5			dB	
Transmitter and Dispersion Penalty (TDP), Each Lane	TDP			2.9	dB	
Side Mode Suppression Ratio	SMSR	30			dB	
Average Launch Power of OFF Transmitter	Poff			-30	dBm	
RIN OMA	TX ΔTJ			-128	dB/HZ	
Transmitter Reflectance				-12	dB	
Optical Return Loss Tolerance	ORL			20	dB	
Optical Output Eye	Compliant with PSM4 MSA {0.31, 0.4, 0.45, 0.34, 0.38, 0.4}					

Parameter		Symbol	Min.	Typ.	Max.	Unit	Notes
Receiver							
Signaling Speed (100PPM, Per Lane)"		B		25. 78125		Gb/s	
Lane Wavelengths		λ	1295	1310	1325	Nm	
Average Receive Power (Per Lane)			-12 .66		2	dBm	2
Rx OMA(Per Lane)					2.2	dBm	
Difference in Receiver Power Between Any Two Lanes (OMA)					5	dB	
Sensitivity in OMA (Per lane)		P_{min}			-11.35	dB	3
Damage Threshold			3			dBm	
Stressed Sensitivity in OMA Per Lane)					-8.' 79	dBm	
Conditions of Stressed Receiver Sensitivity Test:							
Vertical Eye Closure Penalty, Each Lane		VECP	1.9			dB	
Stressed Eye J2 Jitter, Each Lane			0.27			UI	
Stressed Eye J4 Jitter, Each Lane			0.39		UI		
Stressed Eye Mask Definition{X1, X2, X3, Y1, Y2, Y3}		{0.24,0.5,0.5,0.24,0.24,0.4}					
Receiver Reflectance					-26	dB	
LOS Hysteresis			0.5		6	dB	
LOS Thds	**Increasing Light Input**	P_{los+}			-12	dBm	4
	Decreasing Light Input	P_{los-}	-20			dBm	

Notes:

1. Average launch power is informative and not the principal indicator of signal strength. A transmitter with launch power below the min value cannot be compliant; however, a value above it does not ensure compliance.
2. Average receive power is informative and not the principal indicator of signal strength. A received power below the min value cannot be compliant; however, a value above it does not ensure compliance.
3. Specified at BER of 5x10-5.
4. In average power.



X1	X2	X3	Y1	Y2	Y3	Max Hit Ratio
0.31	0.4	0.45	0.34	0.38	0.4	5x10^(-5)

Figure 2 Optical Output Eye Diagram

V. CONTROL INTERFACE

Two-Wire Management Interface

The QSFP28 Module supports alarm, control and monitor functions via a two-wire interface bus. Upon module initialization, these functions are available. QSFP28 two-wire electrical interface consists of 2 pins of SCL (2-wire serial interface clock) and SDA (2-wire serial interface data).

Parameter	Symbol	Min	Typical	Max	Units	Notes
SCL and SDA	V_{OL}	0		0.4	V	1
	V_{OH}	Vcc-0.5		Vcc+0.3	V	
	V_{IL}	-0.3		Vcc*0.3	V	
	V_{IH}	Vcc*0.7		Vcc+0.5	V	
LPMode, Reset and ModSelL	V_{IL}	-0.3		0.8	V	
	V_{IH}	2		Vcc+0.3	V	
ModPrsL and IntL	V_{OL}	0		0.4	V	
	V_{OH}	Vcc-0.5		Vcc+0.3	V	

Notes:

1. IOL (max) =3.0mA; Capacitance for SCL and SDA I/O pin less than 14pF; Total bus capacitive load for SCL and SDA less than 100pF with maximum 3.0kΩ pull-up resistor (less than 200pF with maximum 1.6kΩ pull-up resistor).

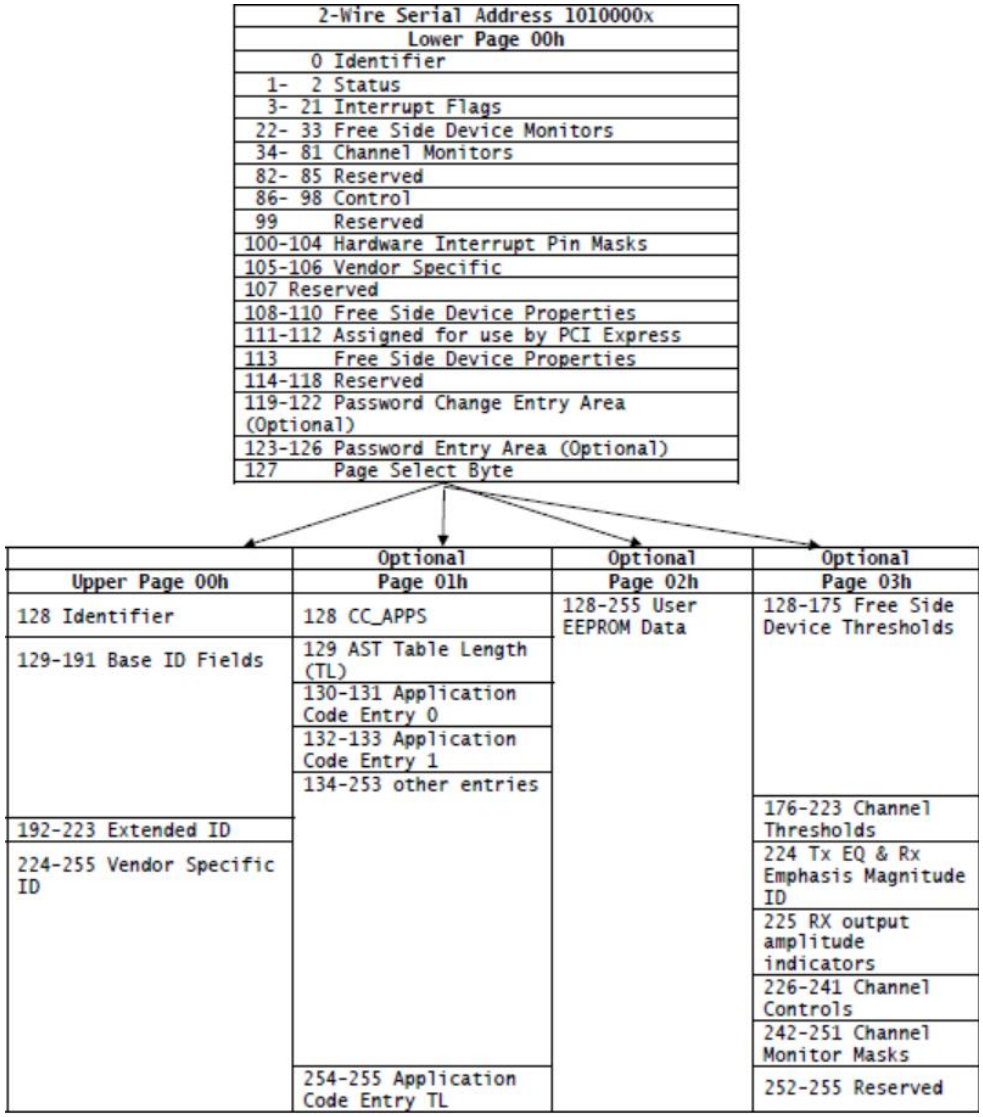


Figure 2 – Two-Wire Interface Fields

The operating and diagnostics information is monitored and reported by a Digital Diagnostics Transceiver Controller (DDTC) inside the transceiver, which is accessed through a 2-wire serial interface. The 2-wire serial interface shall consist of a master and slave. The fixed side shall be the master and the free side shall be the slave. Control and data are transferred serially. The master shall initiate all data transfers. Data can be transferred from the master to the slave and from the slave to the master. The 2-wire interface shall consist of clock (SCL) and data (SDA) signals. The master utilizes SCL to clock data and control information on the 2-wire bus. The master and slave shall latch the state of SDA on the positive transitioning edge of SCL. The SDA signal is bi-directional. During data transfer, the SDA signal shall transition when SCL is low. A transition on the SDA signal while SCL is high shall indicate a stop or start condition.

VI. PIN ASSIGNMENT

Pin	Logic	Symbol	Name/Description
1	GND	GND	Ground
2	CML-I	Tx2n	Transmitter Inverted Data Input
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input
4	GND	GND	Ground
5	CML-I	Tx4n	Transmitter Inverted Data Input
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input
7	GND	GND	Ground
8	LVTTL-I	ModSell	Module Select
9	LVTTL-I	Resetl .	Module Reset
10	VCC	Vcc_ Rx	+3.3V Power supply receiver
11	LVCMOS_I/O	SCL	2-wire serial interface clock
12	L VCMOS-I/O	SDA	2-wire serial interface data
13	GND	GND	Ground
14	CML-O	Rx3p	Receiver Non-Inverted Data Output
15	CML-O	Rx3n	Receiver Inverted Data Output
16	GND	GND	Ground
17	CML-O	Rx1p	Receiver Non-Inverted Data Output
18	CML-O	Rx1n	Receiver Inverted Data Output
19	GND	GND	Ground

VI. PIN ASSIGNMENT

Pin	Logic	Symbol	Name/Description
20	GND	GND	Ground
21	CML-O	Rx2n	Receiver Inverted Data Output
22	CML-O	Rx2p	Receiver Non-Inverted Data Output
23	GND	GND	Ground
24	CML-O	Rx4n	Receiver Inverted Data Output
25	CML-O	Rx4p	Receiver Non-Inverted Data Output
26	GND	GND	Ground
27	LVTTL-O	ModPrsL	Module Present, Grounded Inside the Module
28	LVTTL-O	IntL	Interrupt
29	VCC	VCC Tx	+3.3 V Power Supply Transmitter
30	VCC	VCC1	+3.3V Power Supply
31	LVTTL-I	L PMode	Low Power Mode, Active High
32	GND	GND	Ground
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input
34	CML-I	Tx3n	Transmitter Inverted Data Input
35	GND	GND	Ground
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input
37	CML-I	Tx1n	Transmitter Inverted Data Input
38	GND	GND	Ground

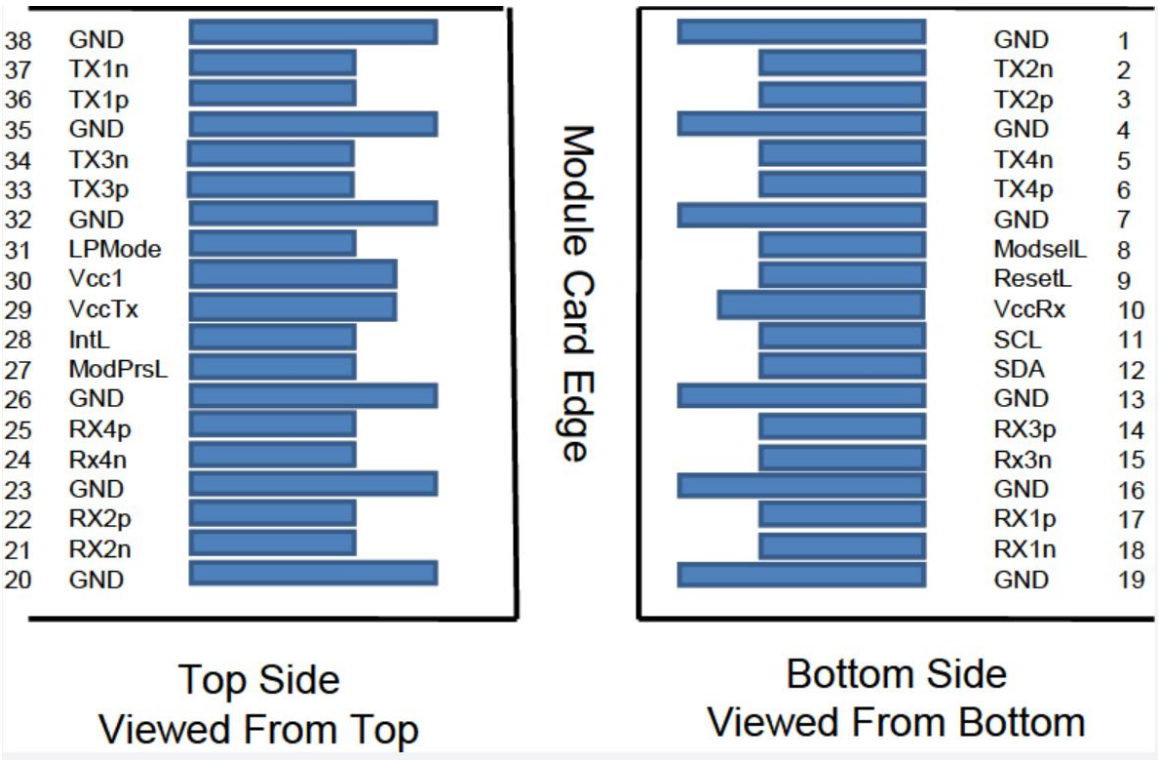


Figure 3 Pin Configuration

VII. MECHANICAL DIMENSIONS

Unit: mm

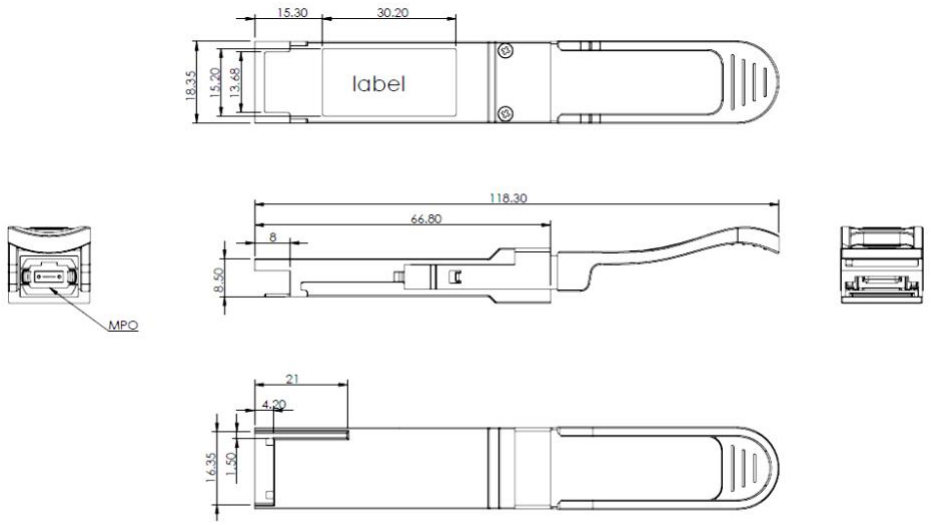


Figure 4 Mechanical Dimensions

To minimize MPO connection induced reflections, an MPO receptacle with 8-degree angled end-face is utilized for this product. A female MPO connector with 8-degree end-face should be used with this product as illustrated in below.

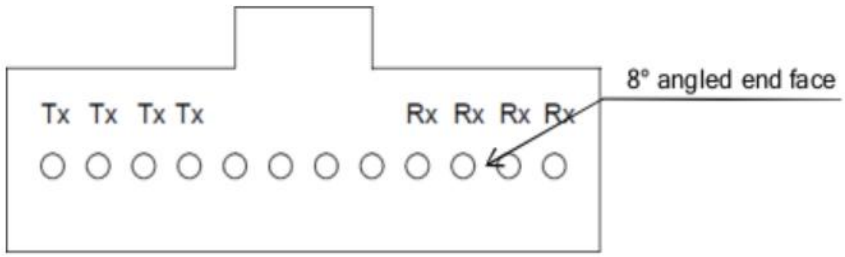


Figure 5 Optical Interface

VIII. REGULATORY COMPLIANCE

Certification	Standard
EMC/EMI	FCC Part 15, Subpart B (Class B) EN55032 (Class B)
ESD	EN61000-4-2, Criterion B JEDEC JESD22-A114-B Human Body Model
Laser Safety	21 CFR 1040.10 and 1040.11 Except for Conformance with IEC 60825-1 Ed. 3. described in Laser Notice No. 56, dated May 8, 2019.
Environmental RoHS 6 ISA S71.04 G2	RoHS 6 ISA S71.04 G2

CAUTION: Use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.

Attention – L'utilisation des commandes ou réglages ou l'exécution des procédures autres que celles spécifiées dans les présentes exigences peuvent être la cause d'une exposition à un rayonnement dangereux.

REFERENCES

1. 100G PSM4 MSA Technical Specification 2. IEEE Std 802.3bm-2015
3. SFF-8665 Rev 1.9 June 29, 2015
4. SFF-8636 Rev 2.9 April 21, 2017
5. SFF-8679 Rev 1.7 August 12, 2014