QSFP28 100GBASE-LR4 1310nm 10km Industrial Transceiver

QSFP28-LR4-XCVR-I-LL

Application

- 100GBASE-LR4 100G Ethernet, Telecom

Features

- Compliant with QSFP28 Standard:SFF-8665 Revision 1.9, SFF-8636 Revision 2.6
- Compliant with IEEE 802.3ba 100GBASE-LR4
- High speed I/O electrical interface (CAUI-4) compliant with IEEE 802.3bm
- Maximum power consumption 4.5W
- -40~85 ºC Case Operating Temperature
- LAN WDM EML laser and PIN Receiver Array
- QSFP28 MSA package with duplex LC connector
- Two Wire Serial Interface with Digital Diagnostic Monitoring
- Complies with EU Directive 2011/65/EU (RoHS compliant)
- Single 3.3V Supply Voltage
- Class 1 Laser

Product Specifications

I. Absolute Maximum Ratings

Parameter	Symbol	Min	Typ.	Max	Unit	Ref.
Storage Temperature	Ts	-40		+85	℃	
Supply Voltage	Vcc	-0.5		3.6	V	
Operating Humidity (non-condensing)	RH	5		95	%	
Data Input Voltage – Differential	$\|V_{DIP}-V_{DIN}\|$			1.0	V	
Control Input Voltage	V_1	-0.3		Vcc+0.5	V	
Control Output Current	I_o	-20		20	mA	

II. Recommended Operating Environment

Parameter	Symbol	Min	Typ.	Max	Unit	Ref.
Operating Case Temperature	T_{OPR}	-40		85	℃	
Power Supply Voltage	Vcc	3.135	3.3	3.465	V	
Instantaneous peak current at hot plug	$I_{CC\ IP}$			1800	mA	Per pin
Sustained peak current at hot plug	$I_{CC\ SP}$			1485	mA	Per pin
Maximum Power Dissipation	P_{DLP}			4.5	W	
Maximum Power Dissipation, Low Power Mode	P_{DLP}			1.5	W	
Aggregate Bit Rate	ABR		103.125		Gb/s	
Data Rate per Lane	DRL		25.78		Gb/s	

Control Input Voltage High	V_{IH}	V_{CC}*0.7		V_{CC}+0.3	V	
Control Input Voltage Low	V_{IL}	-0.3		V_{CC}*0.3	V	
Two Wire Serial Interface Clock Rate				400	kHz	
Power Supply Noise				66	mVpp	10Hz -10MHz
Rx Differential Data Output Load			100		ohms	
Operating Distance		2		10000	m	

III. Optical Characteristics

Parameter	Symbol	Min	Typ.	Max	Unit	Ref.
Transmitter						
Wavelength L0	λ_{C0}	1294.53	1295.56	1296.59	nm	
Wavelength L1	λ_{C1}	1299.02	1300.05	1301.09	nm	
Wavelength L2	λ_{C2}	1303.54	1304.58	1305.63	nm	
Wavelength L3	λ_{C3}	1308.09	1309.14	1310.19	nm	
Side-mode suppression ratio	SMSR	30			dB	
Total Average Optical Launch Power	P_{OUT}			10.5	dBm	
Average Launch Power Tx_Off (Each Lane)	P_{OUT_OFF}			-30	dBm	
Average Optical Launch Power (Each Lane)	P_{OUTL}	-4.3		4.5	dBm	
Extinction Ratio	ER	4			dB	
Spectral Width	$\Delta\lambda$			1	nm	

Optical Modulation Amplitude (Each Lane)	OMA	-1.3		4.5	dBm	
Launch Power in OMA minus TDP (Each Lane)	OMA-TDP	-2.3			dBm	
Difference in launch power between any two lanes (OMA)	DT_OMA			5	dB	
Transmitter and Dispersion Penalty (Each Lane)	TDP			2.2	dB	
Optical Return Loss Tolerance	ORLT			20	dB	
Transmitter Eye Mask Definition			IEEE 802.3ba-2010			
Relative Intensity Noise	RIN			-130	dB/Hz	

Receiver

Wavelength L0	λ_{C0}	1294.53	1295.56	1296.59	nm	
Wavelength L1	λ_{C1}	1299.02	1300.05	1301.09	nm	
Wavelength L2	λ_{C2}	1303.54	1304.58	1305.63	nm	
Wavelength L3	λ_{C3}	1308.09	1309.14	1310.19	nm	
Receiver Sensitivity (OMA) per Lane				-8.6	dBm	
Stressed Receiver Sensitivity in OMA (Each Lane)				-6.8	dBm	
Stressed Receiver Sensitivity Test Conditions:						
Stressed Eye J2 Jitter (Each Lane)			0.3		UI	
Stressed Eye J9 Jitter (Each Lane)			0.47		UI	
Vertical Eye Closure Penalty			1.8		dB	
Damage Threshold for Receiver	$P_{in,\ damage}$	5.5			dBm	
Average Receive Power (Each Lane)		-10.6		4.5	dBm	

Receive Power in OMA (Each Lane), Overload	OMA			4.5	dBm	
Difference in receive power between any two lanes (OMA)	DR_OMA			5.5	dB	
Receiver 3dB electrical upper cut-off frequency (each lane)	F_C			31	GHz	
Receiver Reflectance	RX_R			-26	dB	

Note:

1. Measured with a PRBS2^{31}-1 test pattern @25.78125Gbps, BER≦10^{-12}

IV. Electrical Characteristics

High-Speed Signal: Compliant to CAUI-4 (IEEE 802.3bm)

Low-Speed Signal: Compliant to SFF-8679

Parameter	Symbol	Min	Typ.	Max	Unit	Ref.
Transmitter						
Differential Data Input Amplitude	$V_{IN,P-P}$	95		900	mVpp	1
Differential Termination Mismatch				10	%	
LPMode, Reset and ModSelL	V_{IL}	-0.3		0.8	V	
	V_{IH}	2		V_{CC}+0.3	V	
Receiver						
Differential Data Output Amplitude	$V_{OUT,P-P}$	250		900	mVpp	1
Differential Termination Mismatch				10	%	
Output Rise/Fall Time, 20%~80%	T_R	9.5			ps	

ModPrsL and IntL	V_{OL}	0		0.4	V	I_{OL}=4mA
	V_{OH}	V_{CC}-0.5		V_{CC}+0.3	V	I_{OL}=-4mA

Note:

1. Amplitude customization beyond these specs is dependent on validation in customer system.

V. Digital Diagnostic Monitoring Information

Parameter	Range	Accuracy	Unit	Calibration
Temperature	-5 to 85	±3	ºC	Internal
Voltage	0 to V_{CC}	0.1	V	Internal
Tx Bias Current (Each Lane)	0 to 100	10%	mA	Internal
Tx Output Power (Each Lane)	-4.3 to 4.5	±3	dB	Internal
Rx Power (Each Lane)	-10.6 to 4.5	±3	dB	Internal

VI. Timing

Timing for QSFP+ Soft Control and Status Functions

Parameter	Symbol	Min	Typ.	Max	Unit	Ref.
Initialization Time	t_init			10	s	1
Reset Init Assert Time	t_reset_init			50	µs	4
Serial Bus Hardware Ready Time	t_serial			2000	ms	
Monitor Data Ready Time	t_data			2000	ms	

Reset Assert Time	t_reset			5	s	1,3
LPMode Assert Time	ton_LPMode			50	ms	
LPMode De-assert Time	toff_LPMode			10	s	1
IntL Assert Time	ton_IntL			200	ms	
IntL Deassert Time	toff_IntL			500	µs	
Rx LOS Assert Time	ton_lol			100	ms	
Tx Fault Assert Time	ton_Txfault			200	ms	
Flag Assert Time	ton_flag			200	ms	
Mask Assert Time	ton_mask			100	ms	
Mask Deassert Time	toff_mask			100	ms	
Application or Rate Select Change Time	t_ratesel			N/A	ms	2
Power_over-ride or Power-set Assert Time	ton_Pdown			100	ms	
Power_over-ride or Power-set De-assert Time	toff_Pdown			10	s	1

Notes:

1. Required for temperature stabilization; measured at room temperature condition.
2. This feature is unsupported.
3. Maximum reset hold time 100ms. If exceeded, reset assert time will be equal to initialization time.
4. A reset is generated by a low level longer than t_reset_init present on the ResetL input.

Timing for Squelch & Disable

Parameter	Symbol	Min	Typ.	Max	Unit	Ref.
Rx Squelch Assert Time	ton_Rxsq			80	µs	
Rx Squelch Deassert Time	toff_Rxsq			80	µs	

Tx Squelch Assert Time	ton_Txsq			400	ms	1
Tx Squelch Deassert Time	toff_Txsq			400	ms	1
Tx Disable Assert Time	ton_txdis			100	ms	
Tx Disable Deassert Time	toff_txdis			400	ms	
Rx Output Disable Assert Time	ton_rxdis			100	ms	
Rx Output Disable Deassert Time	toff_rxdis			100	ms	
Squelch Disable Assert Time	ton_sqdis			100	ms	
Squelch Disable Deassert Time	toff_sqdis			100	ms	

Note:

1. Not implemented by default. This feature is configurable at factory, if enabled module power consumption will increase.

Ⅶ. Pin Description

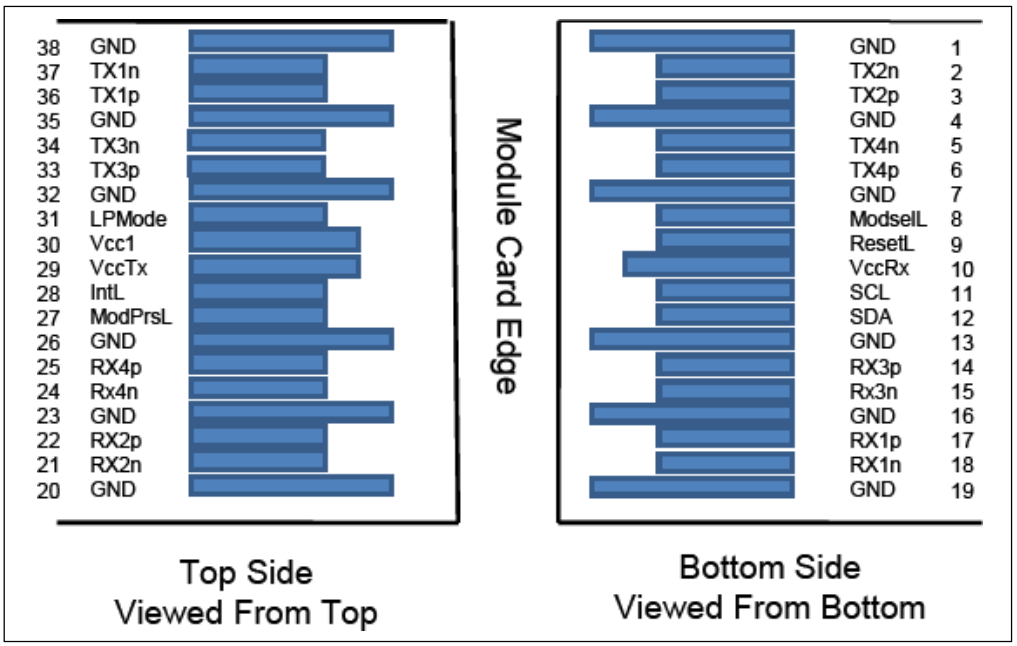

Figure 1 – QSFP+ Module Pad Layout

Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3	
4		GND	Ground	1	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3	
7		GND	Ground	1	1
8	LVTTL-I	ModSelL	Module Select	3	
9	LVTTL-I	ResetL	Module Reset	3	
10		Vcc Rx	+3.3 V Power Supply Receiver	2	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3	
13		GND	Ground	1	1

14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3	
15	CML-O	Rx3n	Receiver Inverted Data Output	3	
16		GND	Ground	1	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3	
18	CML-O	Rx1n	Receiver Inverted Data Output	3	
19		GND	Ground	1	1
20		GND	Ground	1	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3	
23		GND	Ground	1	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3	
26		GND	Ground	1	1
27	LVTTL-O	ModPrsL	Module Present	3	
28	LVTTL-O	IntL	Interrupt	3	
29		Vcc Tx	+3.3V Power supply transmitter	2	2
30		Vcc1	+3.3V Power supply	2	2
31	LVTTL-I	LPMode	Low Power Mode	3	
32		GND	Ground	1	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3	
35		GND	Ground	1	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3	

38		GND	Ground	1	1

Notes:

1. GND is the symbol for signal and supply (power) common for the QSFP+ module. All are common within the QSFP+ module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.
2. Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently.

Ⅷ. Recommended Boot-up Sequence

1. Host asserts LPMode input.
2. Host powers up module and module will be held in low power mode.
3. Host brings up PHY/MAC/PCS and makes sure RF signal is transmitted towards module (Comment: RF signal can be offered anywhere during boot-up.)
4. (Optional) Host checks Initialization Complete Flag (byte 06 bit 0). When "1" is read, module enters low power mode.
5. Host de-asserts LPMode input and writes "1" to High_Power_Class_En bit (byte 93 bit 2), the module will enter high power mode.
6. Host delay t_init (2s).
7. Host checks Initialization Complete Flag (byte 06 bit 0). After entering high power mode, this bit will be "1" and cleared after read. The typical timing is 5s and longest timing under extreme conditions can be up to 60s. If no "1" is read, the boot-up has failed.
8. Host reads interrupt flags (A0.02-0E including Data_Not_Ready flag and all of the interrupt flags) to clear IntL output during initialization.

Note:

1. The requirement of SFF-8636 v1.9 and higher versions is ignored and the module will boot up in high power mode regardless of power consumption.

IX. Diagram Mechanical Drawing