

# QSFP28 100GBASE-SR4 850nm 100m Transceiver

QSFP-100G-SR4-S-LL



## Application

- 100GBASE-SR4 100G Ethernet

## Features

- Hot Pluggable QSFP28 form factor
- Supports 103.1Gb/s aggregate bit rate
- Maximum link length of 100m on OM4 Multimode Fiber (MMF)
- Single MPO12 receptacle
- Single 3.3V power supply
- Typical Power dissipation <1.8W
- 4x25Gb/s 850nm VCSEL-based transmitter
- 4x25G electrical interface
- Commercial operating case temperature range: 0° C to 70° C
- I2C management interface
- RoHS-6 compliant

## Product Specifications

### I. Absolute Maximum Ratings

Parameter	Symbol	Unit	Min	Max
Storage Temperature Range	T <sub>s</sub>	°C	-40	85
Relative Humidity (non-condensing)	RH	%	5	95
Supply Voltage	V <sub>cc</sub>	V	-0.5	3.6

### II. Recommended Operating Conditions

Parameter	Symbol	Min	Type	Max	Unit	Notes
Operating Case Temperature	TOPR	0		70	°C	
Relative Humidity (non-condensing)	RH	5		85	%	
Power Supply Voltage	V <sub>cc</sub>	3.135	3.3	3.465	V	
Total Power Consumption	P <sub>c</sub>			2.5	W	
Supply current				750	mA	
Operating Distance				70	m	OM3
				100	m	OM4

### III. Electrical Characteristics (T<sub>c</sub>=-40°C to 85°C and V<sub>cc</sub>= 3.135 to 3.465V)

Parameter	Unit	Symbol	Min	Type	Max
Supply Voltage	V	V <sub>cc</sub>	3.135		3.465

<b>Supply Current</b>	A	I <sub>cc</sub>			1.5
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<b>Module total power</b>	W	P		1.8	
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**Transmitter**

<b>Signaling rate per lane</b>	Gb/s		25.78125 ± 100ppm		
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<b>Differential pk-pk input voltage tolerance</b>	mV	V <sub>in pp diff</sub>			900
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<b>Single-ended voltage tolerance</b>	v	V <sub>in pp</sub>	-0.35		3.3
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<b>Module stress input test</b>			Per Section 83E.3.4.1, IEEE 802.3 bm		
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**Receiver**

<b>Signaling rate per lane</b>	Gb/s		25.78125 ± 100ppm		
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			100		400
<b>Differential data output swing</b>	mVpp	V <sub>out pp</sub>	300		600
			400		800
			600		1200

<b>Eye width</b>	Ui		0.57		
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<b>Eye height, differential</b>	mV		288		
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<b>Vertical eye closure</b>	dB	VEC	5.5		
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<b>Transition time(20% to 80%)</b>	ps	tr <sub>tf</sub>	12		
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**NOTE:**

1.Maximum total power value is specified across the full operational temperature and voltage range when CDRs are locked or a lack of input signal results in squelch being activated If incorrect frequencies cause the CDRs to continuously attempt to lock maximum power dissipation may reach 4.5W

2.Output voltage is settable in 4 discrete ranges via I2C Default range is Range2.Output voltag

**IV. Transmitter Optical Specifications**

Parameter	Symbol	Min	Type	Max	Unit	Notes
<b>Center Wavelength</b>	$\lambda_C$	840	850	860	nm	
<b>Data rate per lane</b>	DR		25.78125		Gbps	
<b>Optical Power for TX DISABLE</b>				30	dBm	
<b>Average launch power, each lane</b>	$P_{avg}$	-8.4		2.4	dBm	
<b>Optical Power OMA, each Lane</b>	POMA	-6.4		3	dBm	
<b>Extinction Ratio</b>	ER	2			dB	
<b>RMS spectral width</b>	$\Delta\lambda$			0.6	nm	
<b>Optical Return Loss Tolerance</b>	ORLT			12	dB	

**V. Receiver Optical Specifications**

Parameter	Symbol	Min	Type	Max	Unit	Notes
<b>Center Wavelength</b>	$\lambda_C$	840	850	860	nm	
<b>Data rate per lane</b>	DR		25.78125		Gbps	
<b>Overload input optical power</b>	RH	2.4				

<b>Stressed receiver sensitivity (OMA),each lane(5E-5)</b>	V <sub>in</sub>			-5.2	dBm	
<b>Rx LOS Assert</b>	T <sub>s</sub>	-30			dBm	
<b>Rx LOS De-assert</b>	V <sub>cc</sub>			-10	dBm	
<b>Rx LOS Hysteresis</b>	R <sub>H</sub>	0.5			dB	

## VI. High Speed Electrical Specifications

Parameter	Min	Type	Max	Unit	Notes
<b>Input differential impedance</b>	90	100	110	Ω	
<b>Differential data input swing</b>	300	25.78125	1100	mV	
<b>Differential data output swing</b>	500		800	mV	
<b>Input Logic Level High</b>	2		V <sub>cc</sub>	V	
<b>Input Logic Level Low</b>	0		0.8	V	
<b>Output Logic Level High</b>	V <sub>cc</sub> -0.5		V <sub>cc</sub>	V	
<b>Output Logic Level Low</b>	0		0.4	V	

## VII. Wire Electrical Specifications

Parameter	Symbol	Min	Max	Unit
<b>Host 2-wire Vcc voltage</b>	V <sub>cc_Host_2w</sub>	3.14	3.46	V

<b>SCL and SDA Voltage</b>	VOL	0	0.4	V
	VOH	$V_{cc\_Host\_2w}-0.5$	$V_{cc\_Host\_2w}+0.3$	V
	VIL		$V_{ccT} * 0.3$	V
	VIH	$V_{ccT} * 0.7$	$V_{ccT} + 0.5$	V
<b>Input current on the SCL and SDA</b>	II	-10	10	mA

### VIII. Wire Timing Specifications

Parameter	Symbol	Min	Max	Unit	Notes
<b>Clock Frequency</b>	fSCL	100	400	kHz	1
<b>Clock Pulse Width Low</b>	tLOW	1.3		us	
<b>Clock Pulse Width High</b>	tHIGH	0.6			
<b>Time bus free before new transmission can start</b>	tBUF	20		us	2
<b>START Hold Time</b>	tHD,STA	0.6		us	
<b>START Set-up Time</b>	tSU,STA	0.6		us	
<b>Data In Hold Time</b>	tHD, DAT	0		us	
<b>Data In Set-up Time</b>	tSU, DAT	0.1		us	
<b>Input Rise Time (100kHz)</b>	tR, 100		1000	ns	3
<b>Input Rise Time (400kHz)</b>	tR, 400		300	ns	3

<b>Input Fall Time (100kHz)</b>	tF, 100	300	ns	4
<b>Input Fall Time (400kHz)</b>	tF, 400	300	ns	4
<b>STOP Set-up Time</b>	tSU, STO	0.6		

**Notes:**

1. Module shall operate with fSCL up to 100 kHz without requiring clock stretching. The module may clock stretch with fSCL greater than 100 kHz and up to 400 kHz.
2. Between STOP and START and between ACK and ReSTART.
3. From (VIL,MAX-0.15) to (VIH,MIN+0.15).
4. From (VIH,MIN+0.15) to (VIL,MAX-0.15).

### IX.Memory Specifications

Parameter	Symbol	Min	Max	Unit	Notes
<b>Serial Interface Clock Holdoff "Clock Stretching"</b>	T_clock_hold		500	us	1
<b>Complete Single or Sequential Write up to 4 Byte</b>	tWR		40	ms	
<b>Complete Sequential Write of 5~8 Byte</b>	tWR		80	ms	
<b>Endurance (Write Cycles)</b>		10k		cycles	

**NOTE:**

1. Maximum time the QSFP28 module may hold the SCL line low before continuing with a read or write operation.

### X. Digital Diagnostics Monitor Accuracy

Parameter	Accuracy	Unit	Calibration
<b>Temperature</b>	± 3	°C	Internal
<b>Voltage</b>	± 3	%	Internal
<b>Tx Bias Current (Each Lane)</b>	10	%	Internal

<b>Tx Output Power (Each Lane)</b>	±3	dB	Internal
<b>Rx Power (Each Lane)</b>	±3	dB	Internal

### XI. Pin Definitions

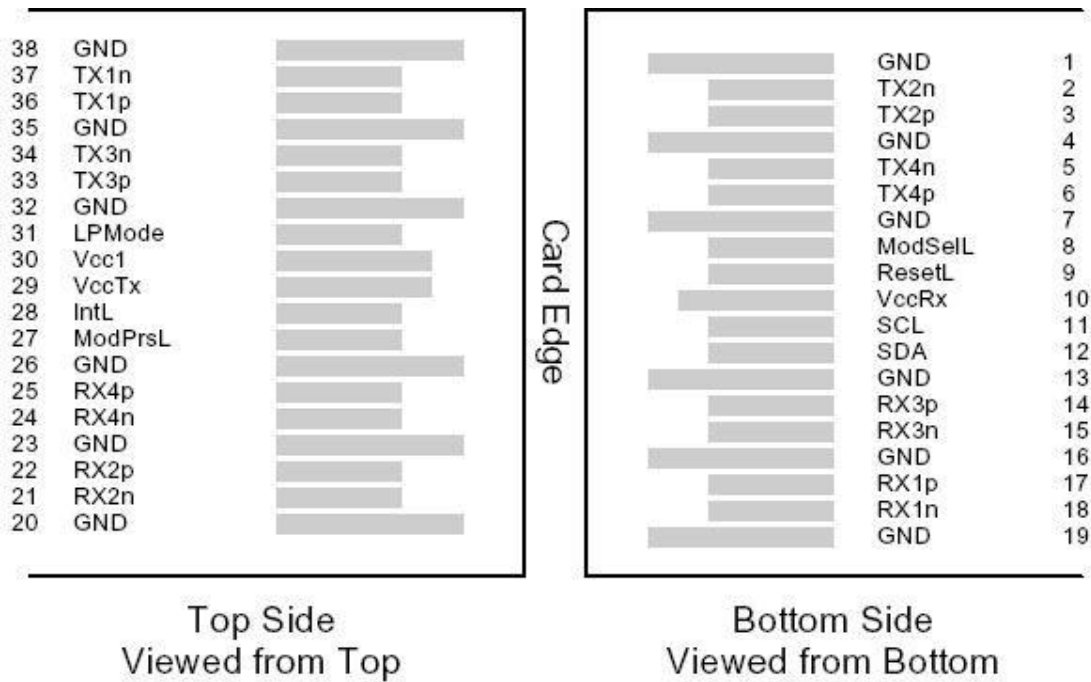


Figure 1 – QSFP28-compliant 38-pin connector (per SFF-8679)

Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3	
4		GND	Ground	1	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3	



<b>7</b>		GND	Ground	<b>1</b>	<b>1</b>
<b>8</b>	LVTTTL-I	ModselL	Module Select	<b>3</b>	
<b>9</b>	LVTTTL-I	ResetL	Module Reset	<b>3</b>	
<b>10</b>		Vcc Rx	+3.3V Power Supply Receiver	<b>2</b>	<b>2</b>
<b>11</b>	LVC MOS-I/O	SCL	2-wire serial interface clock	<b>3</b>	
<b>12</b>	LVC MOS-I/O	SDA	2-wire serial interface data	<b>3</b>	
<b>13</b>		GND	Ground	<b>1</b>	<b>1</b>
<b>14</b>	CML-O	Rx3p	Receiver Non-Inverted Data Output	<b>3</b>	
<b>15</b>	CML-O	Rx3n	Receiver Inverted Data Output	<b>3</b>	
<b>16</b>		GND	Ground	<b>1</b>	<b>1</b>
<b>17</b>	CML-O	Rx1p	Receiver Non-Inverted Data Output	<b>3</b>	
<b>18</b>	CML-O	Rx1n	Receiver Inverted Data Output	<b>3</b>	
<b>19</b>		GND	Ground	<b>1</b>	<b>1</b>
<b>20</b>		GND	Ground	<b>1</b>	<b>1</b>
<b>21</b>	CML-O	Rx2n	Receiver Inverted Data Output	<b>3</b>	
<b>22</b>	CML-O	Rx2p	Receiver Non-Inverted Data Output	<b>3</b>	
<b>23</b>		GND	Ground	<b>1</b>	<b>1</b>
<b>24</b>	CML-O	Rx4n	Receiver Inverted Data Output	<b>3</b>	

25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3	
26		GND	Ground	1	1
27	LVTTTL-O	ModPrsL	Module Present	3	
28	LVTTTL-O	IntL	Interrupt	3	
29		Vcc Tx	+3.3V Power supply transmitter	2	2
30		Vcc1	+3.3V Power supply	2	2
31	LVTTTL-I	LPMode	Low Power Mode	3	
32		GND	Ground	1	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3	
35		GND	Ground	1	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3	
38		GND	Ground	1	1

**Note1:**

GND is the symbol for signal and supply (power) common for the QSFP+ module. All are common within the QSFP+ module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

**Note2:**

Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently.

## IV. Mechanical Specifications

The mechanical specifications are compliant to the QSFP28 transceiver module specifications.

