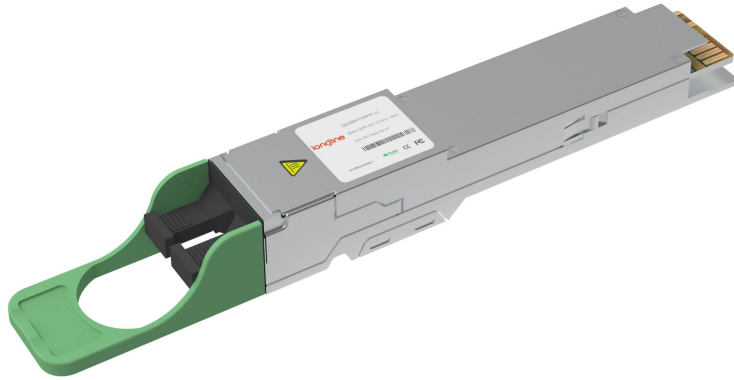


# 800GBASE-2LR4 QSFP-DD 1310nm 10km Dual CS Transceiver

QDD800-PLR8-B1-LL



## Application

- 800G Ethernet
- Data Center
- Breakout 2x 400G LR4

## Features

- Case Operating Temperature 0~ 70°C
- Two Wire Serial Interface with Digital Diagnostic Monitoring
- Class 1 Laser

## Standards

- Compliant with MSA:
  - 2x400G-LR4-10 Optical Interface
- Compliant with IEEE P802.3ck D3.0
  - 2x400GAUI-4 C2M Electrical Interface
- Compliant with QSFP-DD800 MSA HW Rev 6.01 Type 2A with Dual CS Connector
- Compliant with CMIS Rev 5.0

## Description

Longline's 800GBASE-2LR4 QSFP-DD transceiver supports up to 10km link lengths over single-mode fiber (SMF) via dual CS connectors. This transceiver is compliant with IEEE P802.3ck D3.0, QSFP-DD800 MSA HW Rev 6.01 and CMIS Rev 5.0 standard. The built-in digital diagnostics monitoring (DDM) allows access to real-time operating parameters. It is suitable for 800G Ethernet, Data Center, Breakout 2x 400G LR4 application.

## Products Specifications

### I. Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
<b>Storage Temperature</b>	$T_S$	-40	85	°C
<b>Supply Voltage</b>	$V_{CC}$	-0.5	3.6	V
<b>Relative Humidity (Non-condensing)</b>	RH	5	95	%
<b>Data Input Voltage Differential</b>	$ V_{DIP}-V_{DIN} $		1	V
<b>Control Input Voltage</b>	$V_I$	-0.3	$V_{CC}+0.5$	V
<b>Control Output Current</b>	$I_O$	-20	20	mA

### II. Recommended Operating Conditions

Parameter	Symbol	Min.	Typical	Max.	Unit
<b>Operating Case Temperature</b>	$T_{OPR}$	0		70	°C
<b>Power Supply Voltage</b>	$V_{CC}$	3.135	3.3	3.465	V
<b>Instantaneous Peak Current at Hot Plug</b>	$I_{CC\_IP}$			TBD	mA
<b>Sustained Peak Current at Hot Plug</b>	$I_{CC\_SP}$			TBD	mA

Parameter	Symbol	Min.	Typical	Max.	Unit
<b>Maximum Power Dissipation</b>	$P_D$		16.5	18	W
<b>Maximum Power Dissipation, Low Power Mode</b>	$P_{DLP}$			TBD	W
<b>Signalling Speed per Lane</b>	DRL		53.125		GBd
<b>Control Input Voltage High</b>	$V_{IH}$	$V_{CC}*0.7$		$V_{CC}+0.3$	V
<b>Control Input Voltage Low</b>	$V_{IL}$	-0.3		$V_{CC}*0.3$	V
<b>Two Wire Serial Interface Clock Rate</b>				400	kHz
<b>Power Supply Noise 1 kHz -1 MHz (p-p)</b>				66	mVpp
<b>Operating Distance</b>		2		10000	m

### III. Optical Characteristics

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
<b>Transmitter</b>						
<b>Wavelength L0, L4</b>	$\lambda_{C0}, \lambda_{C4}$	1264.5	1271	1277.5	nm	
<b>Wavelength L1, L5</b>	$\lambda_{C1}, \lambda_{C5}$	1284.5	1291	1297.5	nm	
<b>Wavelength L2, L6</b>	$\lambda_{C2}, \lambda_{C6}$	1304.5	1311	1317.5	nm	
<b>Wavelength L3, L7</b>	$\lambda_{C3}, \lambda_{C7}$	1324.5	1331	1337.5	nm	
<b>Side Mode Suppression Ratio</b>	SMSR	30			dB	
<b>Total Average Launch Power(Max.)</b>	$AOP_T$			11.1	dBm	

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
<b>Average Launch Power, each Lane</b>	$AOP_L$	-2.7		5.1	dBm	1
<b>Outer Optical Modulation Amplitude (<math>OMA_{outer}</math>), each Lane for <math>TDECQ &lt; 1.4dB</math> for <math>1.4dB \leq TDECQ \leq 3.4dB</math></b>	$T_{OMA}$	0.3 -1.1 + TDECQ		4.4	dBm	
<b>Difference in Launch Power Between any Two Lanes (<math>OMA_{outer}</math>)</b>	$AOP_d$			4	dB	
<b>Transmitter and Dispersion Eye Closure for PAM4 (TDECQ), each Lane</b>	TDECQ			3.9	dB	
<b>Transmitter Eye Closure for PAM4 (TECQ), each Lane</b>	TECQ			3.9	dB	
<b> TDECQ-TECQ </b>				2.5	dB	
<b>Over/Under-shoot</b>				25	%	
<b>Transmitter Power Excursion</b>				5.2	dBm	
<b>Average Launch Power of OFF Transmitter, each Lane</b>	$T_{OFF}$			-16	dBm	
<b>Extinction Ratio</b>	ER	3.5			dB	
<b>Transmitter Transition Time(Max.)</b>	$T_r$			17	ps	
<b><math>RIN_{15.6OMA}</math></b>	RIN			-136	dB/Hz	
<b>Optical Return Loss Tolerance</b>	ORL			15.6	dB	
<b>Transmitter Reflectance</b>	TR			-26	dB	2
<b>Receiver</b>						
<b>Wavelength L0, L4</b>	$\lambda_{C0}, \lambda_{C4}$	1264.5	1271	1277.5	nm	
<b>Wavelength L1, L5</b>	$\lambda_{C1}, \lambda_{C5}$	1284.5	1291	1297.5	nm	
<b>Wavelength L2, L6</b>	$\lambda_{C2}, \lambda_{C6}$	1304.5	1311	1317.5	nm	

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
<b>Wavelength L3, L7</b>	$\lambda_{C3}, \lambda_{C7}$	1324.5	1331	1337.5	nm	
<b>Damage Threshold, each Lane</b>	AOP <sub>D</sub>	6.1			dBm	
<b>Average Receive Power, each Lane</b>	AOP <sub>R</sub>	-9		5.1	dBm	
<b>Receive Power (OMA<sub>outer</sub>), each Lane</b>	OMA <sub>R</sub>			4.4	dBm	
<b>Difference in Receive Power Between any Two Lanes (OMA<sub>outer</sub>)</b>	AOP <sub>g</sub>			4.3	dB	
<b>Receiver Reflectance</b>	RR			-26	dB	
<b>Receiver Sensitivity (OMA<sub>outer</sub>), each Lane for TECQ &lt; 1.4dB for 1.4dB ≤ TECQ ≤ 3.4dB</b>	S <sub>OMA</sub>			-6.8-8.2+TECQ	dBm	
<b>Stressed Receiver Sensitivity (OMA<sub>outer</sub>), each Lane</b>	SRS			-4.3	dBm	3

#### Conditions of Stressed Receiver Sensitivity Test

<b>Stressed Eye Closure for PAM4 (SECQ), Lane Under Test</b>			3.9		dB	
<b>OMA<sub>outer</sub> of each Aggressor Lane</b>			-0.4		dBm	

#### Notes

1. Average launch power, each lane (min) is informative and not the principal indicator of signal strength.
2. Transmitter reflectance is defined looking into the transmitter.
3. Measured with conformance test signal at TP3 for the BER = 2.4x10<sup>-4</sup>.

## IV. Electrical Characteristics

### 1. Electrical Specification High Speed Signal (Compliant with IEEE802.3ck C2M)

Parameter	Symbol	Min.	Typical	Max.	Unit
-----------	--------	------	---------	------	------

#### Receiver (Module Output, TP4)

<b>AC Common-mode Output Voltage (RMS)</b>				25	mV
<b>Differential Peak-to-peak Output Voltage</b>	<b>Short Mode</b>			600	mV
	<b>Long Mode</b>			845	mV
<b>Eye Height</b>	EH	15			mV
<b>Vertical Eye Closure</b>	VEC			12	dB
<b>Common-mode to Differential-mode Return Loss</b>	RLD <sub>c</sub>		802.3ck 120G-1		dB
<b>Effective Return Loss</b>	ERL	8.5			dB
<b>Differential Termination Mismatch</b>				10	%
<b>Transition Time</b>		8.5			ps
<b>DC Common-mode Voltage Tolerance</b>		-0.35		2.85	V

#### Transmitter (Module Input, TP1)

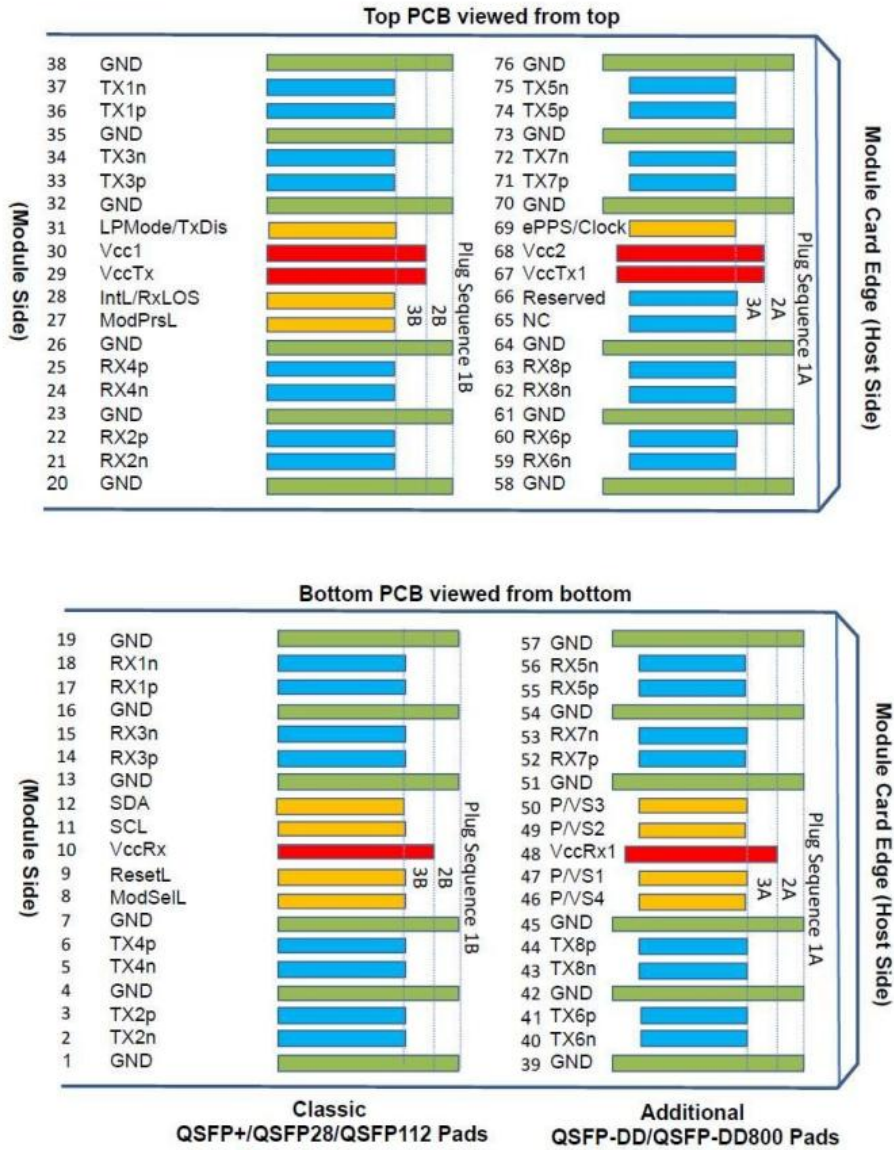
<b>Differential Pk-pk Input Voltage Tolerance (TP1a)</b>		750			mV
<b>AC Common-mode RMS Voltage Tolerance (TP1a)</b>		25			mV
<b>Differential-mode to Common-mode Return Loss</b>	RLcd		802.3ck 120G-2		dB
<b>Effective Return Loss</b>	ERL	8.5			dB

Parameter	Symbol	Min.	Typical	Max.	Unit
<b>Differential Termination Mismatch</b>				10	%
<b>Single-ended Voltage Tolerance Range</b>		-0.4		3.3	V
<b>DC Common-mode Voltage Tolerance</b>		-0.35		2.85	V

## 2. Electrical Specification Low Speed Control and Sense Signals (Compliant with QSFP-DD HW Rev6.01 )

Parameter	Symbol	Min.	Max.	Unit
<b>Module Output SCL and SDA</b>	$V_{OL}$	0	0.4	V
<b>Module Input SCL and SDA</b>	$V_{IL}$	-0.3	$V_{CC} * 0.3$	V
	$V_{IH}$	$V_{CC} * 0.7$	$V_{CC} + 0.5$	V
<b>InitMode, ResetL and ModSelL</b>	$V_{IL}$	-0.3	0.8	V
	$V_{IH}$	2	$V_{CC} + 0.3$	V
<b>IntL</b>	$V_{OL}$	0	0.4	V
	$V_{OH}$	$V_{CC} - 0.5$	$V_{CC} + 0.3$	V

### V. Pin Description



Pin	Logic	Symbol	Description
1		GND	Ground
2	CML-I	Tx2n	Transmitter Inverted Data Input
3	CML-I	Tx2p	Transmitter Non-inverted Data Input
4		GND	Ground



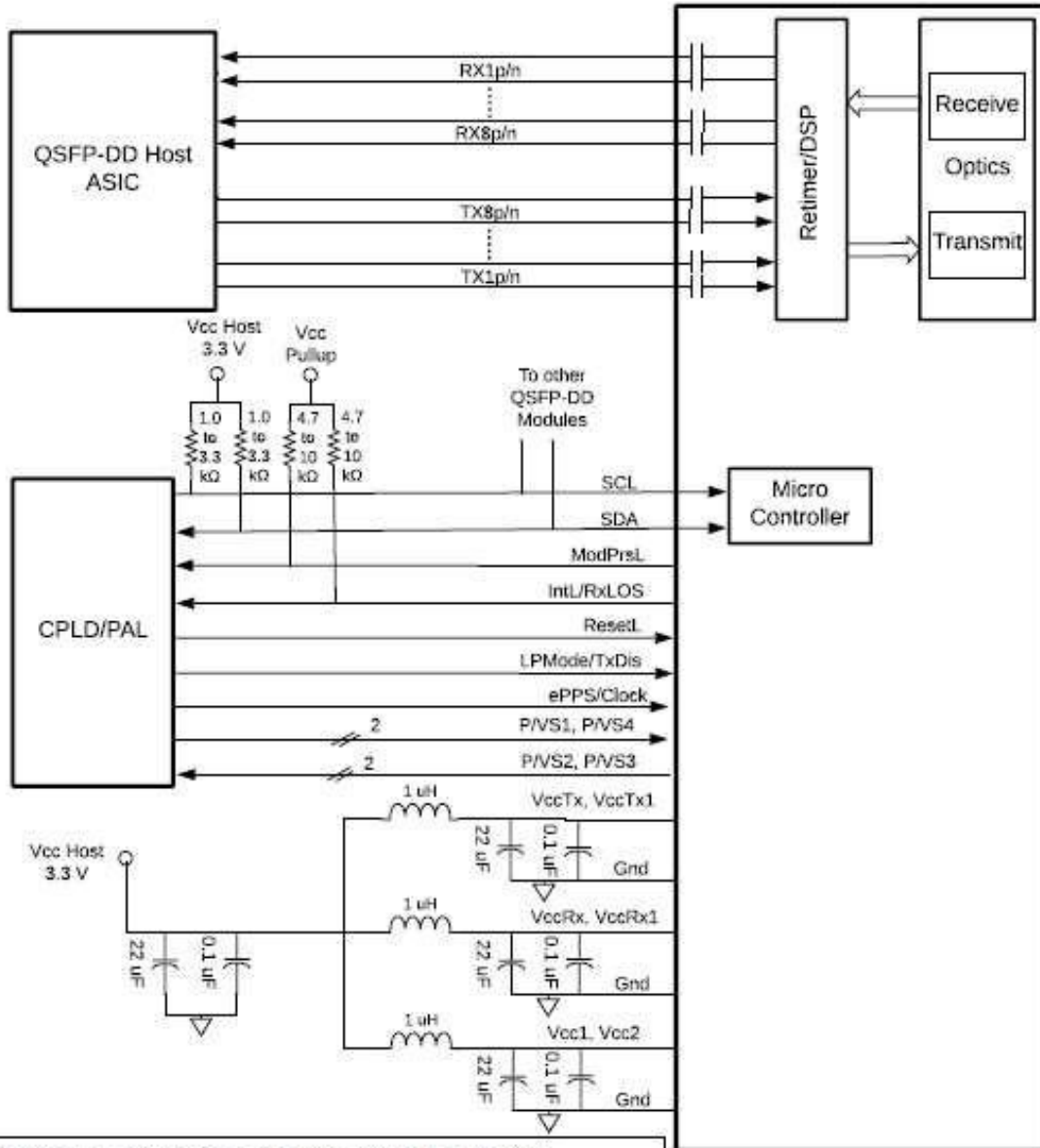
Pin	Logic	Symbol	Description
5	CML-I	Tx4n	Transmitter Inverted Data Input
6	CML-I	Tx4p	Transmitter Non-inverted Data Input
7		GND	Ground
8	LVTTTL-I	ModSelL	Module Select
9	LVTTTL-I	ResetL	Module Reset
10		V <sub>cc</sub> Rx	3.3V Power Supply Receiver
11	LVCNOS-I/O	SCL	TWI Serial Interface Clock
12	LVCNOS-I/O	SDA	TWI Serial Interface Data
13		GND	Ground
14	CML-O	Rx3p	Receiver Non-inverted Data Output
15	CML-O	Rx3n	Receiver Inverted Data Output
16		GND	Ground
17	CML-O	Rx1p	Receiver Non-inverted Data Output
18	CML-O	Rx1n	Receiver Inverted Data Output
19		GND	Ground
20		GND	Ground
21	CML-O	Rx2n	Receiver Inverted Data Output
22	CML-O	Rx2p	Receiver Non-inverted Data Output

Pin	Logic	Symbol	Description
23		GND	Ground
24	CML-O	Rx4n	Receiver Inverted Data Output
25	CML-O	Rx4p	Receiver Non-inverted Data Output
26		GND	Ground
27	LVTTL-O	ModPrsL	Module Present
28	LVTTL-O	IntL/RxLOS	Interrupt/Optional Rx LOS
29		V <sub>cc</sub> Tx	3.3V Power Supply Transmitter
30		V <sub>cc</sub> 1	3.3V Power Supply
31	LVTTL-I	LPMode/TxDis	Low Power Mode/Optional TX Disable
32		GND	Ground
33	CML-I	Tx3p	Transmitter Non-inverted Data Input
34	CML-I	Tx3n	Transmitter Inverted Data Input
35		GND	Ground
36	CML-I	Tx1p	Transmitter Non-inverted Data Input
37	CML-I	Tx1n	Transmitter Inverted Data Input
38		GND	Ground
39		GND	Ground
40	CML-I	Tx6n	Transmitter Inverted Data Input

Pin	Logic	Symbol	Description
41	CML-I	Tx6p	Transmitter Non-inverted Data Input
42		GND	Ground
43	CML-I	Tx8n	Transmitter Inverted Data Input
44	CML-I	Tx8p	Transmitter Non-inverted Data Input
45		GND	Ground
46	LVC MOS/CML-I	P/VS4	Programmable/ Module Vendor Specific 4
47	LVC MOS/CML-I	P/VS1	Programmable/ Module Vendor Specific1
48		V <sub>cc</sub> Rx1	3.3V Power Supply
49	LVC MOS/CML-O	P/VS2	Programmable/ Module Vendor Specific2
50	LVC MOS/CML-O	P/VS3	Programmable/ Module Vendor Specific 3
51		GND	Ground
52	CML-O	Rx7p	Receiver Non-inverted Data Output
53	CML-O	Rx7n	Receiver Inverted Data Output
54		GND	Ground
55	CML-O	Rx5p	Receiver Non-inverted Data Output
56	CML-O	Rx5n	Receiver Inverted Data Output
57		GND	Ground
58		GND	Ground

Pin	Logic	Symbol	Description
59	CML-O	Rx6n	Receiver Inverted Data Output
60	CML-O	Rx6p	Receiver Non-inverted Data Output
61		GND	Ground
62	CML-O	Rx8n	Receiver Inverted Data Output
63	CML-O	Rx8p	Receiver Non-inverted Data Output
64		GND	Ground
65		NC	Not Connected
66		Reserved	
67		V <sub>cc</sub> Tx1	3.3V Power Supply
68		V <sub>cc</sub> 2	3.3V Power Supply
69	LVCML-I	ePPS/Clock	1PPS PTP Clock or Reference Clock Input
70		GND	Ground
71	CML-I	Tx7p	Transmitter Non-inverted Data Input
72	CML-I	Tx7n	Transmitter Inverted Data Input
73		GND	Ground
74	CML-I	Tx5p	Transmitter Non-inverted Data Input
75	CML-I	Tx5n	Transmitter Inverted Data Input
76		GND	Ground

## VI. Recommended QSFP-DD/QSFP-DD800 Host Board Schematic



**QSFP-DD/QSFP-DD800  
Optical Module**

Note: Filter capacitors values are informative and application dependent, 0.1 µF capacitors should be placed in close proximity to power pads and may be duplicated for individual pads to provide additional high frequency filtering.

Note: Vcc1/Vcc2 may be connected to VccTx/VccTx1 or VccRx/VccRx1 within the module provided the applicable derating of the maximum current limit is used.

### VII. Digital Diagnostic Functions

Parameter	Range	Accuracy	Unit	Calibration
Temperature	0~70	±3	°C	Internal
Voltage	0~V <sub>CC</sub>	0.1	V	Internal
Tx Bias Current (each Lane)	0~100	10%	mA	Internal
Tx Output Power (each Lane)	-2.7~5.1	±3	dB	Internal
Rx Receive Power (each Lane)	-9~5.1	±3	dB	Internal

### VIII. Diagram Mechanical Drawing

unit: mm

