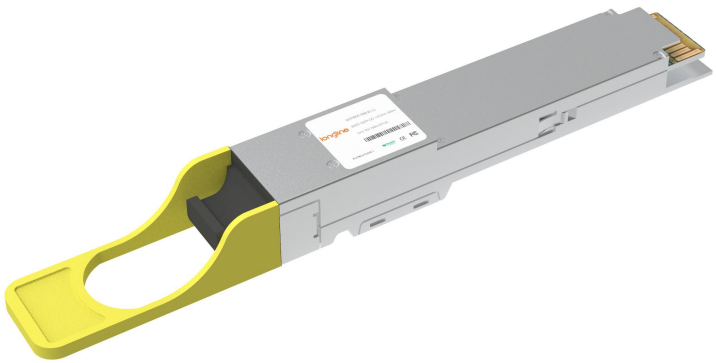
800GBASE-2FR4 QSFP-DD PAM4 1310nm 2km DOM Dual CS SMF Optical Transceiver Module

QDD800-DR8-B1-LL



Application

- 200G Ethernet
- 2x400GBASE-FR4

Features

- Compliant with IEEE 802.3cu-2021: - 2x400GBASE-FR4 Optical Interface
- Compliant with IEEE P802.3ck D2.2: - 2x400GAUI-4 C2M Electrical Interface
- Compliant with QSFP-DD800 MSA HW Rev 6.01 Type 2A with Dual CS Connector
- Compliant with QSFP-DD CMIS Rev 5.0
- Case Operating Temperature 0°C to 70°C
- Two Wire Serial Interface with Digital Diagnostic Monitoring
- Class 1 Laser

Description

The QSFP-DD transceiver supports up to 2km link lengths over single-mode fiber (SMF) via dual CS connectors. This transceiver is compliant with IEE802.3ck, IEEE 802.3cu and QSFP-DD MSA standards. The built-in digital diagnostics monitoring (DDM) allows access to real-time operating parameters. It is suitable for 800G Ethernet, Breakout 2x 400G FR4, Data Center and Cloud Networks.

I. Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Notes
Storage Temperature	TS	-40	85	°C	
Supply Voltage	VCC	-0.5	3.6	V	
Relative Humidity (non-condensing)	RH	5	95	%	
Data Input Voltage Differential	IVDIP-VDINI	-	1	V	
Control Input Voltage	VI	-0.3	VCC+0.5	V	
Control Output Current	IO	-20	20	mA	

II. Electrical Characteristics (TOP = 0 to 70 ° C, VCC = 3.0 to 3.60 Volts)

Parameter	Symbol	Min.	Typical	Max.	Unit	Note
Operating Case Temperature	TOPR	0	-	70	°C	1
Power Supply Voltage	VCC	3.135	3.3	3.465	V	
Instantaneous peak current at hot plug	ICC_IP	-	-	TBD	mA	
Sustained peak current at hot plug	ICC_SP	-	-	TBD	mA	
Maximum Power Dissipation	PD	-	-	TBD	W	
Maximum Power Dissipation, Low Power Mode	PDLP	-	-	TBD	W	
Signalling Speed per Lane	DRL	-	53.125	-	GBd	
Control Input Voltage High	VIH	VCC*0.7	-	VCC+0.3	V	
Control Input Voltage Low	VIL	-0.3	-	VCC*0.3	V	
Two Wire Serial Interface Clock Rate	-	-	-	400	kHz	
Power Supply Noise 1 kHz - 1 MHz (p-p)	-	-	-	66	mVpp	
Operating Distance	-	2	-	2000	m	

Functional Characteristics (Optical)

The following tables list the performance specifications for the various functional blocks of the integrated optical
transceiver module.

III. Optical Parameters(TOP = 0 to 70° C, VCC = 3.00 to 3.60 Volts)

Parameter	Symbol	Min.	Typical	Max.	Unit	Note
Wavelength L0	λC0	1264.5	1271	1277.5	nm	
Wavelength L1	λC1	1284.5	1291	1297.5	nm	
Wavelength L2	λC2	1304.5	1311	1317.5	nm	
Wavelength L3	λC3	1324.5	1331	1337.5	nm	
Side Mode Suppression Ratio	SMSR	30	-	-	dB	
Total average launch power (max)	AOPT			10.4		
Average Launch Power, each lane	AOPL	-3.2	-	4.4	dBm	1
Outer Optical Modulation Amplitude (OMAouter), each Lane for TDECQ <1.4 dB for 1.4 dB ≤TDECQ ≤3.4 dB	TOMA	0.2 –1.6 + TDECQ	-	3.7	dBm	
Difference in launch power between any two lanes (OMAouter) (max)	AOPd			3.9	dB	
Transmitter and Dispersion Eye Closure for PAM4 (TDECQ), each lane	TDECQ	-	-	3.4	dB	
Transmitter eye closure for PAM4 (TECQ), each lane	TECQ	-	-	3.4	dB	
| TDECQ – TECQ |	-	-	-	2.5	dB	
Over/under-shoot	-	-	-	22	%	
Transmitter power excursion	-	-	-	1.8 d	dBm	
Average Launch Power of OFF Transmitter, each lane	TOFF	-	-	-16	dBm	
Extinction Ratio	ER	3.5	-	-	dB	
Transmitter transition time (max)	Tr			17	ps	
RIN17.1OMA (max)	RIN	-	-	-136	dB/Hz	2
Optical Return Loss Tolerance	ORL	-	-	17.1	dB	
Transmitter Reflectance	TR	-	-	-26	dB	

Note 1: Average launch power, each lane (min) is informative and not the principal indicator of signal strength
Note 2: Transmitter reflectance is defined looking into the transmitter

IV. Receiver Optical Specifications at TP3

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Wavelength L0	λC0	1264.5	1271	1277.5	nm	
Wavelength L1	λC1	1284.5	1291	1297.5	nm	
Wavelength L2	λC2	1304.5	1311	1317.5	nm	
Wavelength L3	λC3	1324.5	1331	1337.5	nm	
Damage Threshold, each Lane	AOPD	5.4	-	-	dBm	
Average Receive Power, each Lane	AOPR	7.2	-	4.4	dBm	
Receive Power (OMAouter), each Lane	OMAR	-	-	3.7	dBm	
Difference in receive power between any two lanes (OMAouter) (max)	AOPg	-	-	4.1		
Receiver Reflectance	RR	-	-	-26	dB	
Receiver sensitivity (OMAouter), each lane for TECQ < 1.4 dB for 1.4 dB≤ TECQ ≤3.4 dB	SOMA	-	-	-4.6 –6 + TECQ	dBm	
Stressed Receiver Sensitivity (OMAouter), each Lane	SRS	-	-	-2.6	dBm	1
Conditions of stressed receiver sensitivity test:						
Stressed eye closure for PAM4 (SECQ), lane under test	-	-	3.4	-	dB	
OMAouter of each aggressor lane	-	-	1.4	-	dBm	

Note 1: Measured with conformance test signal at TP3 for the BER = 2.4x10-4

Functional Characteristics (Electrical)

V. Electrical Specification High Speed Signal (compliant with IEEE P802.3ck C2M)

Receiver (Module Output) at TP4						
Parameter	**Symbol**	**Min.**	**Typical**	**Max.**	**Unit**	**Notes**
AC common-mode output Voltage (RMS)		-	-	25	mV	
Differential peak-to-peak output voltage Short mode Long mode		-	-	600 900	mV mV	
Eye height, differential	EH	15	-	-	mV	
Vertical eye closure	VEC	-	-	12	dB	

Common-mode to differential return loss	RLDc		802.3ck 120G-1		dB	
Effective return loss, ERL	ERL	8.5	-	-	dB	
Differential termination mismatch		-	-	10	%	
Transition time (20% to 80%)		8.5	-	-	ps	
DC common-mode voltage		-350	-	2850	mV	
Transmitter (Module Input) at TP1						
Parameter	**Symbol**	**Min.**	**Typical**	**Max.**	**Unit**	**Notes**
Differential pk-pk input Voltage tolerance (TP1a)		900	-	-	mV	
AC common-mode RMS voltage tolerance (TP1a)		25			mV	
Differential to common-mode return loss	RLcd		802.3ck 120G-2		dB	
Effective return loss, ERL	ERL	8.5	-	-	dB	
Differential termination mismatch		-	-	10	%	
Single-ended voltage tolerance range		-0.4	-	3.3	V	
DC common-mode Voltage tolerance		-0.35	-	2.85	V	

VI. – Electrical Specification Low Speed Control and Sense Signals

Parameter	**Symbol**	**Min.**	**Max.**	**Unit**	**Condition**
Module output SCL and SDA	VOL	0	0.4	V	
Module Input SCL and SDA	VIL	-0.3	VCC*0.3	V	
	VIH	VCC*0.7	VCC+0.5	V	
LPMode/TxDis, ResetL and ModSelL	VIL	-0.3	0.8	V	
	VIH	2	VCC+0.3	V	
IntL/RxLos	VOL	0	0.4	V	
	VOH	VCC-0.5	VCC+0.3	V	

Pin Definitions

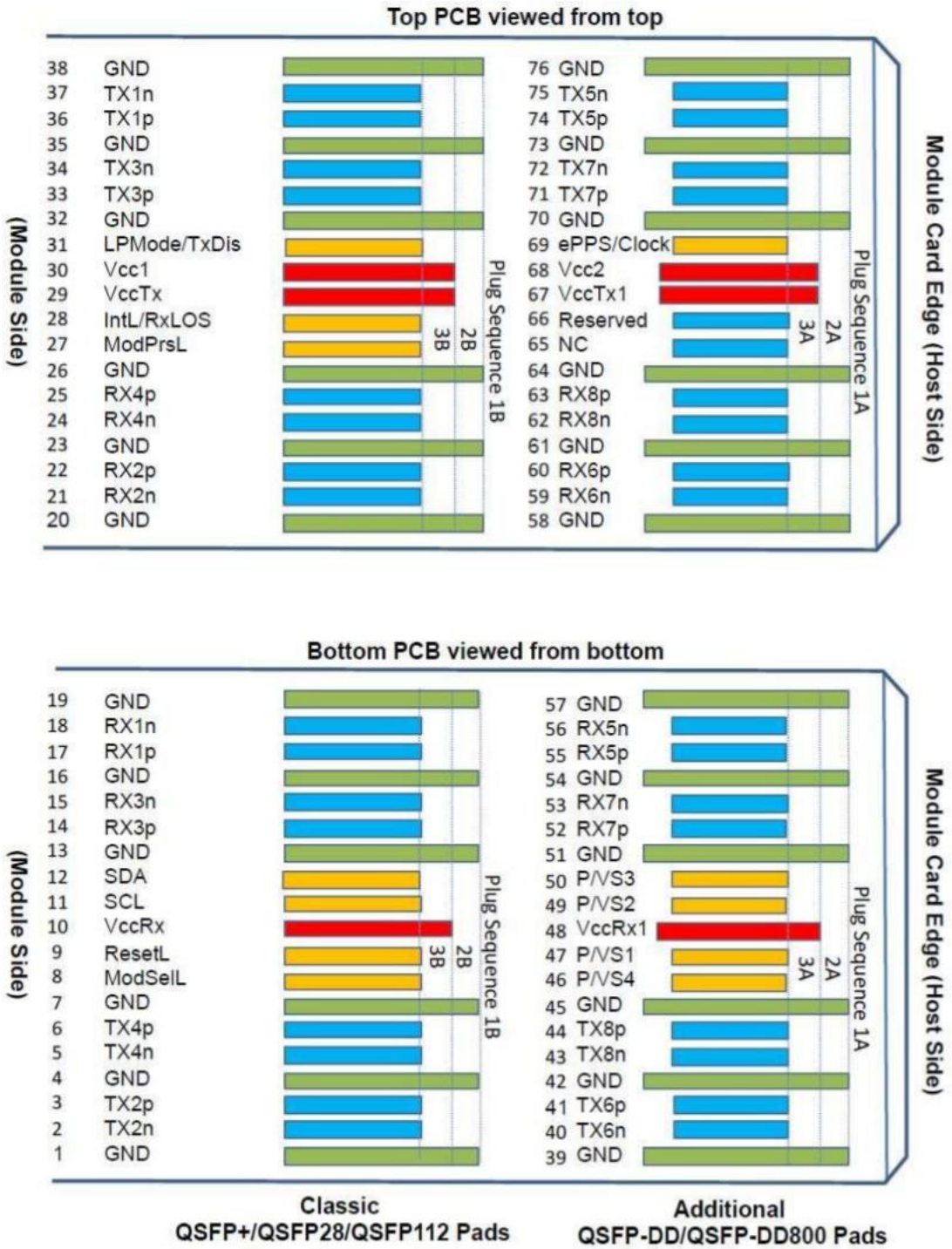
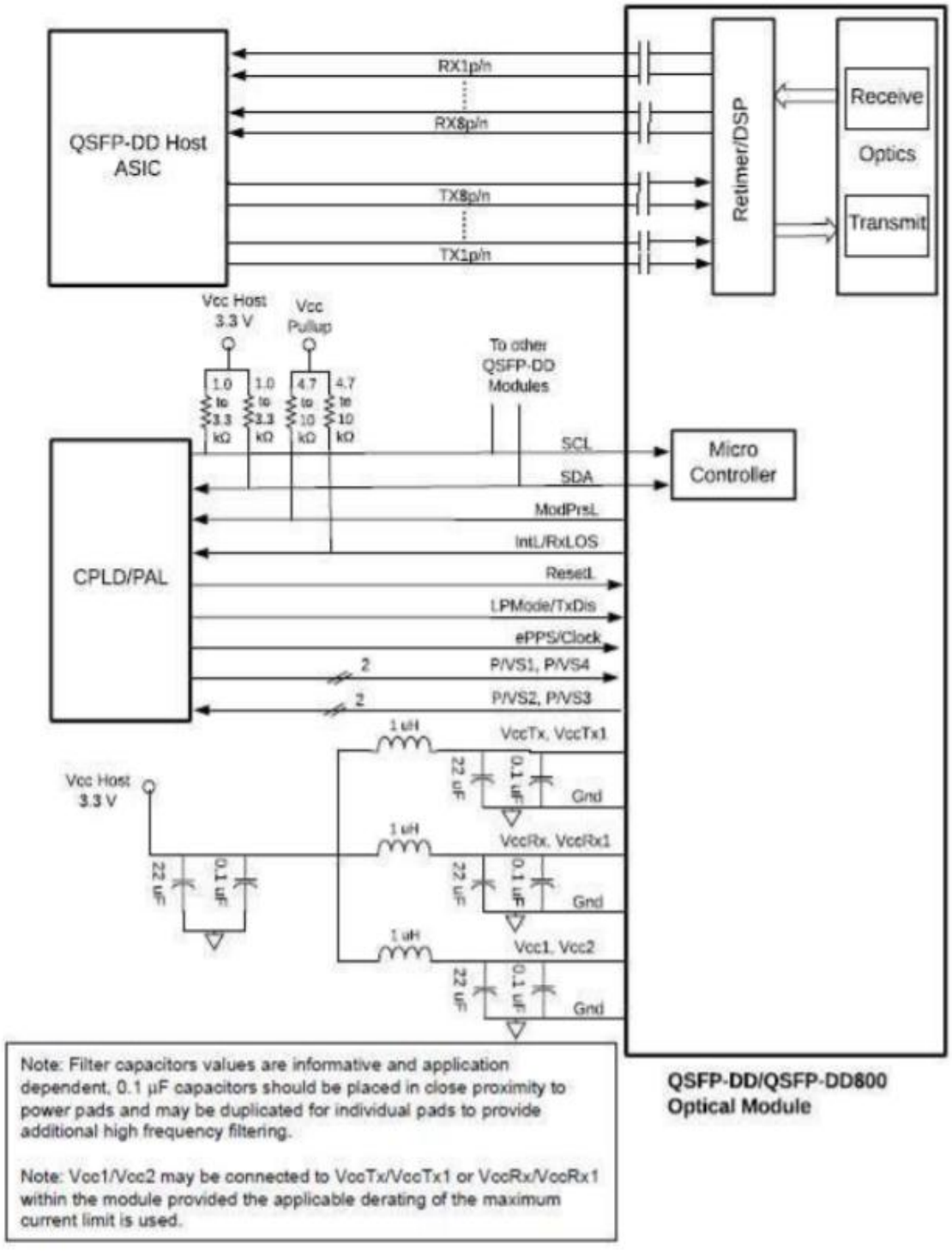


Figure 1 – Pin definitions of the module high speed inputs/outputs

VII. Module Pin Definitions

Pin #	Logic	Symbol	Definition	Pin #	Logic	Symbol	Definition
1		GND	Ground	39		GND	Ground
2	CML-I	Tx2n	Transmitter Inverted Data Input	40	CML-I	Tx6n	Transmitter Inverted Data Input
3	CML-I	Tx2p	Transmitter Non-inverted Data Input	41	CML-I	Tx6p	Transmitter Non-inverted Data Input
4		GND	Ground	42		GND	Ground
5	CML-I	Tx4n	Transmitter Inverted Data Input	43	CML-I	Tx8n	Transmitter Inverted Data Input
6	CML-I	Tx4p	Transmitter Non-inverted Data Input	44	CML-I	Tx8p	Transmitter Non-inverted Data Input
7		GND	Ground	45		GND	Ground
8	LVTTL-I	ModSelL	Module Select	46	LVCMOS/CMLI	P/VS4	Programmable/Module Vendor Specific 4
9	LVTTL-I	ResetL	Module Reset	47	LVCMOS /CML-I	P/VS1	Programmable/Module Vendor Specific 1
10		GND	Ground	48		VccRx1	3.3V Power Supply
11	LVCMOS-I/O	SCL	TWI serial interface clock	49	LVCMO S /CML-O	P/VS2	Programmable/Module Vendor Specific 2
12	LVCMOS-I/O	SDA	TWI serial interface data	50	LVCMO S /CML-O	P/VS3	Programmable/Module Vendor Specific 3
13		GND	Ground	51		GND	Ground
14	CML-O	Rx3p	Receiver Non-inverted Data Output	52	CML-O	Rx7p	Programmable/Module Vendor Specific 2
15	CML-O	Rx3n	Receiver Inverted Data Output	53	CML-O	Rx7n	Programmable/Module Vendor Specific 3
16		GND	Ground	54		GND	Ground
17	CML-O	Rx1p	Receiver Non-inverted Data Output	55	CML-O	Rx5p	Receiver Non-inverted Data Output
18	CML-O	Rx1n	Receiver Inverted Data Output	56	CML-O	Rx5n	Receiver Inverted Data Output
19		GND	Ground	57		GND	Ground
20		GND	Ground	58		GND	Ground
21	CML-O	Rx2n	Receiver Inverted Data Output	59	CML-O	Rx6n	Receiver Inverted Data Output
22	CML-O	Rx2p	Receiver Non-inverted Data Output	60	CML-O	Rx6p	Receiver Non-inverted Data Output
23		GND	Ground	61		GND	Ground
24	CML-O	Rx4n	Receiver Inverted Data Output	62	CML-O	Rx8n	Receiver Inverted Data Output
25	CML-O	Rx4p	Receiver Non-inverted Data Output	63	CML-O	Rx8p	Receiver Non-inverted Data Output
26		GND	Ground	64		GND	Ground
27	LVTTL-O	ModPrsL	Module Present	65		NC	Not connected
28	LVTTL-O	IntL/ RxLOS	Interrupt/optional RxLOS	66		Reserved	
29		VccTx	+3.3V Power Supply Transmitter	67		VccTx1	3.3V Power Supply
30		Vcc1	+3.3V Power Supply	68		Vcc2	3.3V Power Supply
31	LVTTL-I	LPMode/ TxDis	Low Power mode/optional TX Disable	69	LVCMOS-I	ePPS/Clock	1PPS PTP clock or reference clock input
32		GND	Ground	70		GND	Ground
33	CML-I	Tx3p	Transmitter Non-inverted Data Input	71	CML-I	Tx7p	Transmitter Non-inverted Data Input
34	CML-I	Tx3n	Transmitter Inverted Data Input	72	CML-I	Tx7n	Transmitter Inverted Data Input
35		GND	Ground	73		GND	Ground
36	CML-	Tx1p	Transmitter Non-inverted Data Input	74	CML-I	Tx5p	Transmitter Non-inverted Data Input
37	CML-	Tx1n	Transmitter Inverted Data Input	75	CML-I	Tx5n	Transmitter Inverted Data Input
38		GND	Ground	76		GND	Ground

VIII. Recommended QSFP-DD/QSFP-DD800 Host Board Schematic



Note: Filter capacitors values are informative and application dependent, 0.1 µF capacitors should be placed in close proximity to power pads and may be duplicated for individual pads to provide additional high frequency filtering.

Note: Vcc1/Vcc2 may be connected to VccTx/VccTx1 or VccRx/VccRx1 within the module provided the applicable derating of the maximum current limit is used.

IX. Digital Diagnostics

Parameter	Range	Accuracy	Unit	Calibration
Temperature	0 to 70	±3	ºC	Internal
Voltage	0 to VCC	0.1	V	Internal
Tx Bias Current (Each Lane)	0 to 100	10%	mA	Internal
Tx Output Power (Each Lane)	-3.2 to +4.4	±3	dB	Internal
Rx Receive Power (Each Lane)	-7.2 to +4.4	±3	dB	Internal

X. Mechanical Diagram