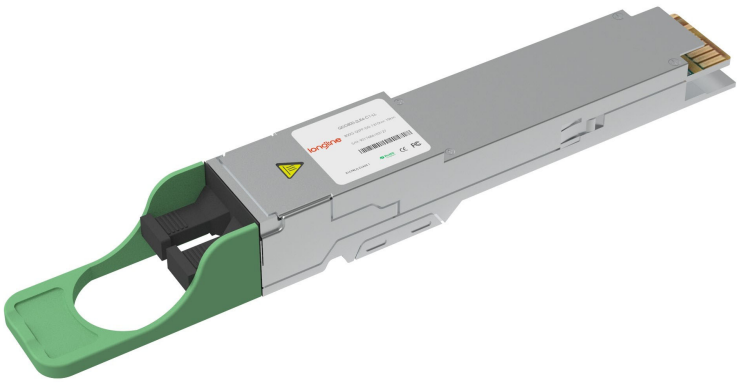
800GBASE-2LR4 QSFP-DD 1310nm 10km Dual CS Transceiver

QDD800-2LR4-C1-LL



Application

- 800G Ethernet
- Data Center
- Breakout 2x 400G LR4

Features

- Case Operating Temperature 0~ 70°C
- Two Wire Serial Interface with Digital Diagnostic Monitoring
- Class 1 Laser

Standards

- Compliant with MSA:
  - 2x400G-LR4-10 Optical Interface
- Compliant with IEEE P802.3ck D3.0
  - 2x400GAUI-4 C2M Electrical Interface
- Compliant with QSFP-DD800 MSA HW Rev 6.01 Type 2A with Dual CS Connector
- Compliant with CMIS Rev 5.0

Description

Longline's 800GBASE-2LR4 QSFP-DD transceiver supports up to 10km link lengths over single-mode fiber (SMF) via dual CS connectors. This transceiver is compliant with IEEE P802.3ck D3.0, QSFP-DD800 MSA HW Rev 6.01 and CMIS Rev 5.0 standard. The built-in digital diagnostics monitoring (DDM) allows access to real-time operating parameters . It is suitable for 800G Ethernet , Data Center , Breakout 2x 400G LR4 application.

Products Specifications

I. Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	T_S	-40	85	°C
Supply Voltage	V_{CC}	-0.5	3.6	V
Relative Humidity (Non-condensing)	RH	5	95	%
Data Input Voltage Differential	IV_{DIP}-$V_{DIN}I$		1	V
Control Input Voltage	V_I	-0.3	V_{CC}+0.5	V
Control Output Current	I_O	-20	20	mA

II. Recommended Operating Conditions

Parameter	Symbol	Min.	Typical	Max.	Unit
Operating Case Temperature	T_{OPR}	0		70	°C
Power Supply Voltage	V_{CC}	3.135	3.3	3.465	V
Instantaneous Peak Current at Hot Plug	I_{CC_IP}			TBD	mA
Sustained Peak Current at Hot Plug	I_{CC_SP}			TBD	mA

Parameter	Symbol	Min.	Typical	Max.	Unit
Maximum Power Dissipation	P_D		16.5	18	W
Maximum Power Dissipation, Low Power Mode	P_{DLP}			TBD	W
Signalling Speed per Lane	DRL		53.125		GBd
Control Input Voltage High	V_{IH}	V_{CC}*0.7		V_{CC}+0.3	V
Control Input Voltage Low	V_{IL}	-0.3		V_{CC}*0.3	V
Two Wire Serial Interface Clock Rate				400	kHz
Power Supply Noise 1 kHz -1 MHz (p-p)				66	mVpp
Operating Distance		2		10000	m

III. Optical Characteristics

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Transmitter						
Wavelength L0, L4	λ_{C0}, λ_{C4}	1264.5	1271	1277.5	nm	
Wavelength L1, L5	λ_{C1}, λ_{C5}	1284.5	1291	1297.5	nm	
Wavelength L2, L6	λ_{C2}, λ_{C6}	1304.5	1311	1317.5	nm	
Wavelength L3, L7	λ_{C3}, λ_{C7}	1324.5	1331	1337.5	nm	
Side Mode Suppression Ratio	SMSR	30			dB	
Total Average Launch Power(Max.)	AOP_T			11.1	dBm	

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Average Launch Power, each Lane	AOP_L	-2.7		5.1	dBm	1
Outer Optical Modulation Amplitude (OMA_{outer}), each Lane for TDECQ<1.4dB for1.4dB<= TDECQ<=3.4dB	T_{OMA}	0.3 –1.1 + TDECQ		4.4	dBm	
Difference in Launch Power Between any Two Lanes (OMA_{outer})	AOP_d			4	dB	
Transmitter and Dispersion Eye Closure for PAM4 (TDECQ), each Lane	TDECQ			3.9	dB	
Transmitter Eye Closure for PAM4 (TECQ), each Lane	TECQ			3.9	dB	
|TDECQ-TECQ|				2.5	dB	
Over/Under-shoot				25	%	
Transmitter Power Excursion				5.2	dBm	
Average Launch Power of OFF Transmitter, each Lane	T_{OFF}			-16	dBm	
Extinction Ratio	ER	3.5			dB	
Transmitter Transition Time(Max.)	Tr			17	ps	
$RIN_{15.6}OMA$	RIN			-136	dB/Hz	
Optical Return Loss Tolerance	ORL			15.6	dB	
Transmitter Reflectance	TR			-26	dB	2
		Receiver				
Wavelength L0, L4	$\lambda_{C0}, \lambda_{C4}$	1264.5	1271	1277.5	nm	
Wavelength L1, L5	$\lambda_{C1}, \lambda_{C5}$	1284.5	1291	1297.5	nm	
Wavelength L2, L6	$\lambda_{C2}, \lambda_{C6}$	1304.5	1311	1317.5	nm	

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Wavelength L3, L7	λ_{C3}, λ_{C7}	1324.5	1331	1337.5	nm	
Damage Threshold, each Lane	AOP_D	6.1			dBm	
Average Receive Power, each Lane	AOP_R	-9		5.1	dBm	
Receive Power (OMA_{outer}), each Lane	OMA_R			4.4	dBm	
Difference in Receive Power Between any Two Lanes (OMA_{outer})	AOP_g			4.3	dB	
Receiver Reflectance	RR			-26	dB	
Receiver Sensitivity (OMA_{outer}),each Lane for TECQ< 1.4dB for 1.4dB≤TECQ≤3.4dB	S_{OMA}			-6.8-8.2+TECQ	dBm	
Stressed Receiver Sensitivity (OMA_{outer}), each Lane	SRS			-4.3	dBm	3
Conditions of Stressed Receiver Sensitivity Test						
Stressed Eye Closure for PAM4 (SECQ), Lane Under Test			3.9		dB	
$OMA_{outer}$of each Aggressor Lane			-0.4		dBm	

Notes

1. Average launch power, each lane (min) is informative and not the principal indicator of signal strength.
2. Transmitter reflectance is defined looking into the transmitter.
3. Measured with conformance test signal at TP3 for the BER = $2.4x10^{-4}$.

IV. Electrical Characteristics

1. Electrical Specification High Speed Signal (Compliant with IEEE802.3ck C2M)

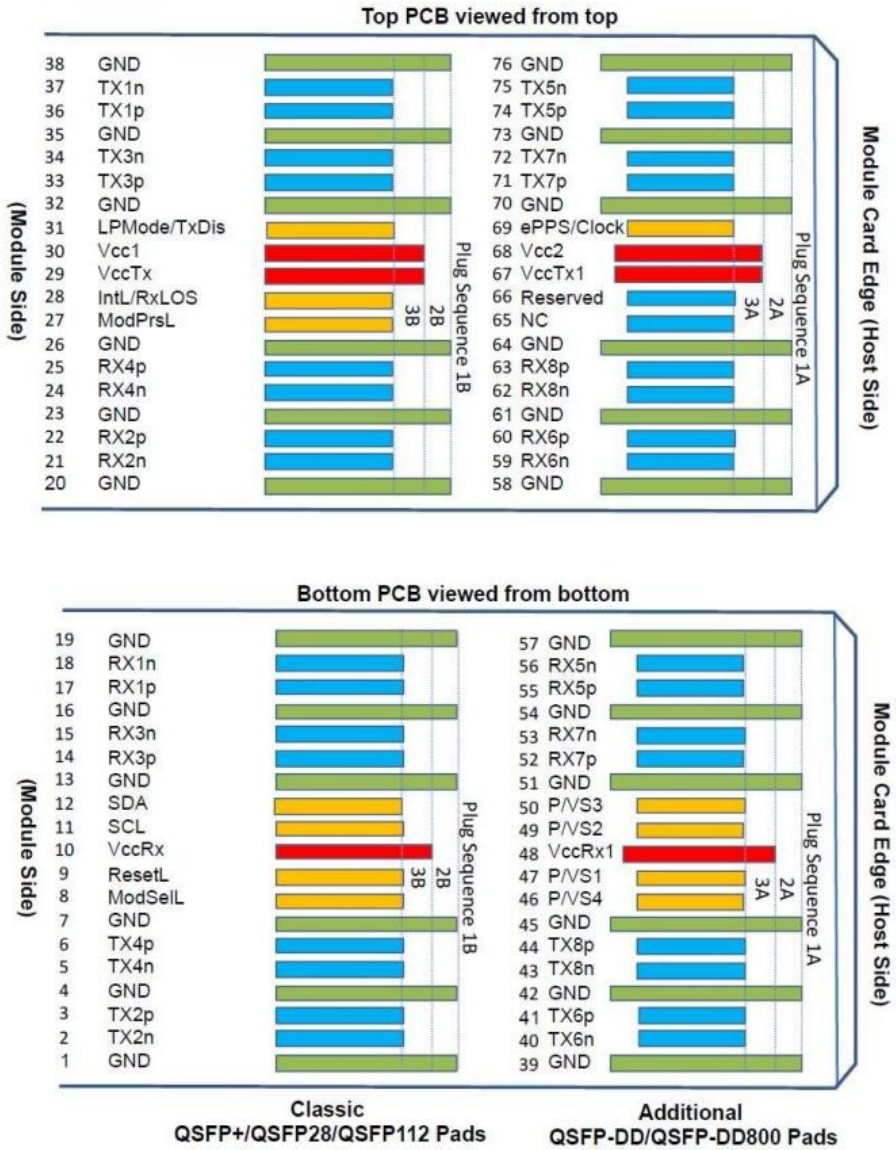
Parameter	Symbol	Min.	Typical	Max.	Unit
Receiver (Module Output, TP4)					
AC Common-mode Output Voltage (RMS)				25	mV
Differential Peak-to-peak Output Voltage — **Short Mode**				600	mV
Differential Peak-to-peak Output Voltage — **Long Mode**				845	mV
Eye Height	EH	15			mV
Vertical Eye Closure	VEC			12	dB
Common-mode to Differential-mode Return Loss	RLD_C		802.3ck 120G-1		dB
Effective Return Loss	ERL	8.5			dB
Differential Termination Mismatch				10	%
Transition Time		8.5			ps
DC Common-mode Voltage Tolerance		-0.35		2.85	V
Transmitter (Module Input, TP1)					
Differential Pk-pk Input Voltage Tolerance (TP1a)		750			mV
AC Common-mode RMS Voltage Tolerance (TP1a)		25			mV
Differential-mode to Common-mode Return Loss	RLcd		802.3ck 120G-2		dB
Effective Return Loss	ERL	8.5			dB

Parameter	Symbol	Min.	Typical	Max.	Unit
Differential Termination Mismatch				10	%
Single-ended Voltage Tolerance Range		-0.4		3.3	V
DC Common-mode Voltage Tolerance		-0.35		2.85	V

2. Electrical Specification Low Speed Control and Sense Signals (Compliant with QSFP-DD HW Rev6.01)

Parameter	Symbol	Min.	Max.	Unit
Module Output SCL and SDA	V_{OL}	0	0.4	V
Module Input SCL and SDA	V_{IL}	-0.3	V_{CC}*0.3	V
	V_{IH}	V_{CC}*0.7	V_{CC}+0.5	V
InitMode, ResetL and ModSelL	V_{IL}	-0.3	0.8	V
	V_{IH}	2	V_{CC}+0.3	V
IntL	V_{OL}	0	0.4	V
	V_{OH}	V_{CC}-0.5	V_{CC}+0.3	V

V. Pin Description



Pin	Logic	Symbol	Description
1		GND	Ground
2	CML-I	Tx2n	Transmitter Inverted Data Input
3	CML-I	Tx2p	Transmitter Non-inverted Data Input
4		GND	Ground

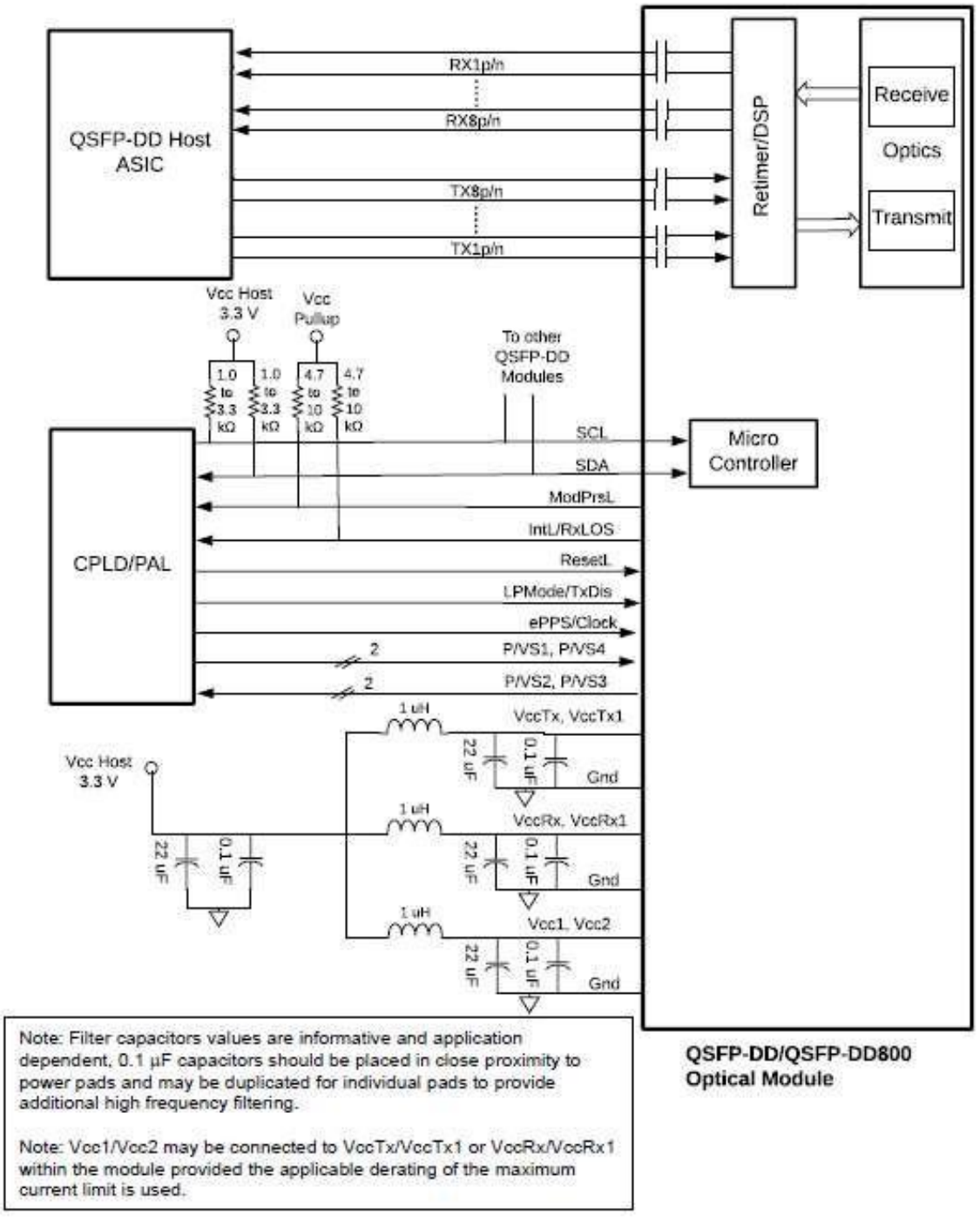
Pin	Logic	Symbol	Description
5	CML-I	Tx4n	Transmitter Inverted Data Input
6	CML-I	Tx4p	Transmitter Non-inverted Data Input
7		GND	Ground
8	LVTTL-I	ModSelL	Module Select
9	LVTTL-I	ResetL	Module Reset
10		$V_{cc}Rx$	3.3V Power Supply Receiver
11	LVCMOS-I/O	SCL	TWI Serial Interface Clock
12	LVCMOS-I/O	SDA	TWI Serial Interface Data
13		GND	Ground
14	CML-O	Rx3p	Receiver Non-inverted Data Output
15	CML-O	Rx3n	Receiver Inverted Data Output
16		GND	Ground
17	CML-O	Rx1p	Receiver Non-inverted Data Output
18	CML-O	Rx1n	Receiver Inverted Data Output
19		GND	Ground
20		GND	Ground
21	CML-O	Rx2n	Receiver Inverted Data Output
22	CML-O	Rx2p	Receiver Non-inverted Data Output

Pin	Logic	Symbol	Description
23		GND	Ground
24	CML-O	Rx4n	Receiver Inverted Data Output
25	CML-O	Rx4p	Receiver Non-inverted Data Output
26		GND	Ground
27	LVTTL-O	ModPrsL	Module Present
28	LVTTL-O	IntL/RxLOS	Interrupt/Optional Rx LOS
29		V_{cc}Tx	3.3V Power Supply Transmitter
30		V_{cc}1	3.3V Power Supply
31	LVTTL-I	LPMode/TxDis	Low Power Mode/Optional TX Disable
32		GND	Ground
33	CML-I	Tx3p	Transmitter Non-inverted Data Input
34	CML-I	Tx3n	Transmitter Inverted Data Input
35		GND	Ground
36	CML-I	Tx1p	Transmitter Non-inverted Data Input
37	CML-I	Tx1n	Transmitter Inverted Data Input
38		GND	Ground
39		GND	Ground
40	CML-I	Tx6n	Transmitter Inverted Data Input

Pin	Logic	Symbol	Description
41	CML-I	Tx6p	Transmitter Non-inverted Data Input
42		GND	Ground
43	CML-I	Tx8n	Transmitter Inverted Data Input
44	CML-I	Tx8p	Transmitter Non-inverted Data Input
45		GND	Ground
46	LVCMOS/CML-I	P/VS4	Programmable/ Module Vendor Specific 4
47	LVCMOS/CML-I	P/VS1	Programmable/ Module Vendor Specific1
48		V_{cc}Rx1	3.3V Power Supply
49	LVCMOS/CML-O	P/VS2	Programmable/ Module Vendor Specific2
50	LVCMOS/CML-O	P/VS3	Programmable/ Module Vendor Specific 3
51		GND	Ground
52	CML-O	Rx7p	Receiver Non-inverted Data Output
53	CML-O	Rx7n	Receiver Inverted Data Output
54		GND	Ground
55	CML-O	Rx5p	Receiver Non-inverted Data Output
56	CML-O	Rx5n	Receiver Inverted Data Output
57		GND	Ground
58		GND	Ground

Pin	Logic	Symbol	Description
59	CML-O	Rx6n	Receiver Inverted Data Output
60	CML-O	Rx6p	Receiver Non-inverted Data Output
61		GND	Ground
62	CML-O	Rx8n	Receiver Inverted Data Output
63	CML-O	Rx8p	Receiver Non-inverted Data Output
64		GND	Ground
65		NC	Not Connected
66		Reserved	
67		V_{cc}Tx1	3.3V Power Supply
68		V_{cc}2	3.3V Power Supply
69	LVCMOS-I	ePPS/Clock	1PPS PTP Clock or Reference Clock Input
70		GND	Ground
71	CML-I	Tx7p	Transmitter Non-inverted Data Input
72	CML-I	Tx7n	Transmitter Inverted Data Input
73		GND	Ground
74	CML-I	Tx5p	Transmitter Non-inverted Data Input
75	CML-I	Tx5n	Transmitter Inverted Data Input
76		GND	Ground

VI. Recommended QSFP-DD/QSFP-DD800 Host Board Schematic



Note: Filter capacitors values are informative and application dependent, 0.1 µF capacitors should be placed in close proximity to power pads and may be duplicated for individual pads to provide additional high frequency filtering.

Note: Vcc1/Vcc2 may be connected to VccTx/VccTx1 or VccRx/VccRx1 within the module provided the applicable derating of the maximum current limit is used.

VII. Digital Diagnostic Functions

Parameter	Range	Accuracy	Unit	Calibration
Temperature	0~70	±3	ºC	Internal
Voltage	0~ V_{CC}	0.1	V	Internal
Tx Bias Current (each Lane)	0~100	10%	mA	Internal
Tx Output Power (each Lane)	-2.7~5.1	±3	dB	Internal
Rx Receive Power (each Lane)	-9~5.1	±3	dB	Internal

VIII. Diagram Mechanial Drawing

unit: mm