

# QSFP-DD 400GBASE-LR8 1310nm 10km Transceiver

QDD-400G-LR8-S-LL



## Application

- 400GBASE-LR8 400G Ethernet
- Data Center

## Features

- Compliant with IEEE 802.3bs standard:
  - 400GBASE-LR8 optical interface
  - 400GAUI-8 electrical interface
- Compliant with QSFP-DD MSA HW Rev 3.0 with duplex LC connector
- Maximum power consumption tbd W
- Case operating temperature 0° C to 70° C
- Two wire serial Interface with digital diagnostic monitoring
- Complies with EU Directive 2011/65/EU (RoHS compliant)
- Class 1 Laser

## Product Specifications

### I. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
<b>Storage Temperature</b>	$T_s$	-40	85	°C	
<b>Supply Voltage</b>	$V_{CC}$	-0.5	3.6	V	
<b>Relative Humidity (non-condensing)</b>	RH	5	95	%	
<b>Data Input Voltage Differential</b>	$ V_{DIP}-V_{DIN} $		1	V	
<b>Control Input Voltage</b>	$V_I$	-0.3	$V_{CC}+0.5$	V	
<b>Control Output Current</b>	$I_o$	-20	20	mA	

### II. Recommended Operating Environment

Parameter	Symbol	Min	Typ.	Max	Unit	Notes
<b>Operating Case Temperature</b>	$T_{OPR}$	0		70	°C	1
<b>Power Supply Voltage</b>	$V_{CC}$	3.135	3.3	3.465	V	
<b>Instantaneous peak current at hot plug</b>	$I_{CC\_IP}$			TBD	mA	
<b>Sustained peak current at hot plug</b>	$I_{CC\_SP}$			TBD	mA	
<b>Maximum Power Dissipation</b>	$P_D$			TBD	W	
<b>Maximum Power Dissipation, Low Power Mode</b>	$P_{DLP}$			TBD	W	
<b>Signalling Speed per Lane</b>	DRL		26.5625		Gbd	
<b>Control Input Voltage High</b>	$V_{IH}$	$V_{CC}*0.7$		$V_{CC}+0.3$	V	
<b>Control Input Voltage Low</b>	$V_{IL}$	-0.3		$V_{CC}*0.3$	V	

<b>Two Wire Serial Interface Clock Rate</b>				400	kHz	
<b>Power Supply Noise</b>				50	mVpp	
<b>Rx Differential Data Output Load</b>			100		Ohm	
<b>Operating Distance</b>		2		10000	m	

### III. Optical Characteristics

The following tables list the performance specifications for the various functional blocks of the integrated optical transceiver module.

Parameter	Symbol	Min	Typ.	Max	Unit	Notes
<b>Transmitter</b>						
<b>Wavelength L0</b>	$\lambda_{C0}$	1272.55	1273.55	1274.54	nm	
<b>Wavelength L1</b>	$\lambda_{C1}$	1276.89	1277.89	1278.89	nm	
<b>Wavelength L2</b>	$\lambda_{C2}$	1281.25	1282.26	1283.27	nm	
<b>Wavelength L3</b>	$\lambda_{C3}$	1285.65	1286.67	1287.68	nm	
<b>Wavelength L4</b>	$\lambda_{C4}$	1294.53	1295.56	1296.59	nm	
<b>Wavelength L5</b>	$\lambda_{C5}$	1299.02	1300.06	1301.09	nm	
<b>Wavelength L6</b>	$\lambda_{C6}$	1303.54	1304.59	1305.63	nm	
<b>Wavelength L7</b>	$\lambda_{C7}$	1308.09	1309.14	1310.19	nm	
<b>Side Mode Suppression Ratio</b>	SMSR	30			dB	
<b>Total Average Launch Power</b>	$AOP_T$			13.2	dBm	
<b>Average Launch Power, each lane</b>	$AOP_L$	-2.8		5.3	dBm	1
<b>Outer Optical Modulation Amplitude (<math>OMA_{outer}</math>), each Lane</b>	$T_{OMA}$	0.2		5.7	dBm	
<b>Difference in Launch Power between any two Lanes (<math>OMA_{outer}</math>)</b>	$D_{T\_OMA}$			4	dB	

<b>Launch Power in OMA<sub>outer</sub> minus TDECQ, each lane for ER&gt; 4.5dB</b>	$T_{OMA-TDECQ}$	-1.2			dBm	
<b>Launch Power in OMA<sub>outer</sub> minus TDECQ, each lane for ER&lt; 4.5dB</b>	$T_{OMA-TDECQ}$	-1.1			dBm	
<b>Transmitter and Dispersion Eye Closure for PAM4 (TDECQ), each lane</b>	TDECQ			3.3	dB	
<b>Average Launch Power of OFF Transmitter, each lane</b>	$T_{OFF}$			-30	dBm	
<b>Extinction Ratio</b>	ER	3.5			dB	
<b>RIN<sub>15.1,OMA</sub></b>	RIN			-132	dB/Hz	
<b>Optical Return Loss Tolerance</b>	ORL			15.1	dB	
<b>Transmitter Reflectance</b>	$T_R$			-26	dB	2

**Notes:**

- Average launch power, each lane (min) is informative and not the principal indicator of signal strength
- Transmitter reflectance is defined looking into the transmitter

Parameter	Symbol	Min	Typ.	Max	Unit	Notes
<b>Receiver</b>						
<b>Wavelength L0</b>	$\lambda_{C0}$	1272.55	1273.55	1274.54	nm	
<b>Wavelength L1</b>	$\lambda_{C1}$	1276.89	1277.89	1278.89	nm	
<b>Wavelength L2</b>	$\lambda_{C2}$	1281.25	1282.26	1283.27	nm	
<b>Wavelength L3</b>	$\lambda_{C3}$	1285.65	1286.67	1287.68	nm	
<b>Wavelength L4</b>	$\lambda_{C4}$	1294.53	1295.56	1296.59	nm	
<b>Wavelength L5</b>	$\lambda_{C5}$	1299.02	1300.06	1301.09	nm	
<b>Wavelength L6</b>	$\lambda_{C6}$	1303.54	1304.59	1305.63	nm	
<b>Wavelength L7</b>	$\lambda_{C7}$	1308.09	1309.14	1310.19	nm	

<b>Damage Threshold, each Lane</b>	AOP <sub>D</sub>	6.3			dBm	
<b>Average Receive Power, each Lane</b>	AOP <sub>R</sub>	-9.1		5.3	dBm	
<b>Receive Power (OMA<sub>outer</sub>), each Lane</b>	OMA <sub>R</sub>			5.7	dBm	
<b>Difference in Receive Power between any two Lanes (OMA<sub>outer</sub>)</b>	D <sub>R_OMA</sub>			4.5	dB	
<b>Receiver Reflectance</b>	RR			-26	dB	
<b>Receiver Sensitivity (OMA<sub>outer</sub>), each Lane</b>	S <sub>OMA</sub>			-7.1	dBm	1
<b>Stressed Receiver Sensitivity (OMA<sub>outer</sub>), each Lane</b>	SRS			-4.7	dBm	2

**Notes:**

- 1.Receiver sensitivity (OMA<sub>outer</sub>), each lane (max) is informative and is defined for a transmitter with SECQ of 0.9 dB
- 2.Measured with conformance test signal at TP3 for the BER =  $2.4 \times 10^{-4}$

## IV. Electrical Characteristics

**Table 1 - Electrical Specification High Speed Signal (compliant with IEEE 802.3bs 400GAUI-8)**

Parameter	Symbol	Min	Typ.	Max	Unit	Notes
<b>Transmitter (Module Input)</b>						
<b>Differential pk-pk input Voltage tolerance</b>		900			mV	
<b>Differential termination mismatch</b>				10	%	
<b>Single-ended voltage tolerance range</b>		-0.4		3.3	V	
<b>DC common mode Voltage</b>		-350		2850	mV	
<b>Receiver (Module Output)</b>						
<b>AC common-mode output Voltage (RMS)</b>				17.5	mV	
<b>Differential output Voltage</b>				900	mV	

<b>Near-end Eye height, differential</b>		70			UI	
<b>Far-end Eye height, differential</b>		30			UI	
<b>Far end pre-cursor ratio</b>				2.5	%	
<b>Differential Termination Mismatch</b>				10	%	
<b>Transition Time (min, 20% to 80%)</b>		9.5			ps	
<b>DC common mode Voltage</b>		-350		2850	mV	

Table 2 - Electrical Specification Low Speed Signal (compliant with QSFP-DD HW Rev 3.0)

Parameter	Symbol	Min	Max	Unit	Condition
<b>Module output SCL and SDA</b>	$V_{OL}$	0	0.4	V	
	$V_{OH}$	$V_{CC}-0.5$	$V_{CC}+0.3$	V	
<b>Module Input SCL and SDA</b>	$V_{IL}$	-0.3	$V_{CC}*0.3$	V	
	$V_{IH}$	$V_{CC}*0.7$	$V_{CC}+0.5$	V	
<b>InitMode, ResetL and ModSelL</b>	$V_{IL}$	-0.3	0.8	V	
	$V_{IH}$	2	$V_{CC}+0.3$	V	
<b>IntL</b>	$V_{OL}$	0	0.4	V	
	$V_{OH}$	$V_{CC}-0.5$	$V_{CC}+0.3$	V	

## V. Digital Diagnostic Monitoring Information

Parameter	Range	Accuracy	Unit	Calibration
<b>Temperature</b>	0 to 70	$\pm 3$	$^{\circ}\text{C}$	Internal
<b>Voltage</b>	0 to $V_{CC}$	0.1	V	Internal
<b>Tx Bias Current (Each Lane)</b>	0 to 100	10%	mA	Internal

<b>Tx Output Power (Each Lane)</b>	-3.5 to +5.3	±3dB	dBm	Internal
<b>Rx Receive Power (Each Lane)</b>	-9.1 to +5.3	±3dB	dBm	Internal

## VI. Pin Definitions

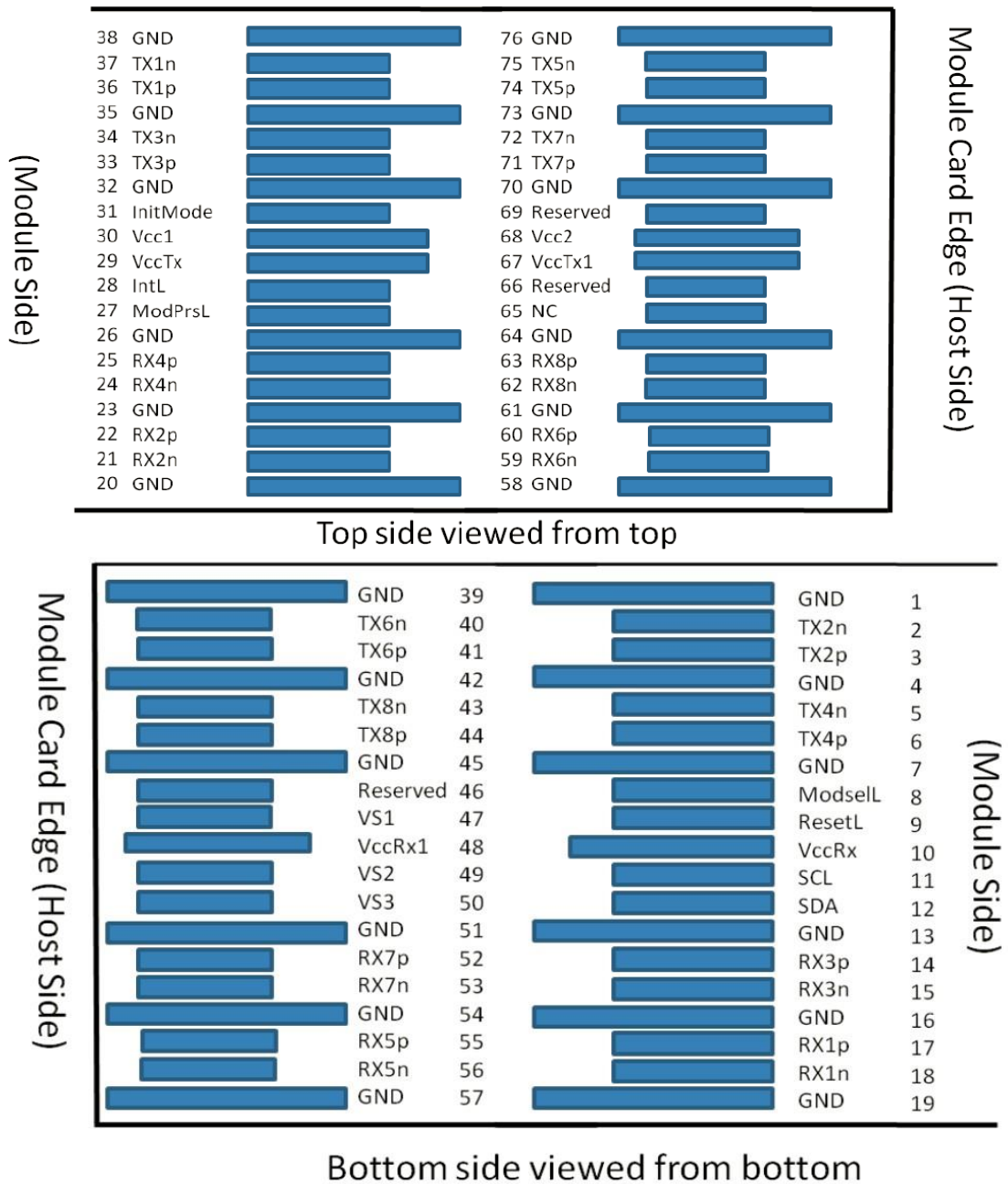


Figure 1 – Pin definitions of the module high speed inputs/outputs

## Pin Definitions

Pin #	Logic	Symbol	Definition
1		GND	Ground
2	CML-I	Tx2n	Transmitter Inverted Data Input
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input
4		GND	Ground
5	CML-I	Tx4n	Transmitter Inverted Data Input
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input
7		GND	Ground
8	LVTTL-I	ModSelL	Module Select
9	LVTTL-I	ResetL	Module Reset
10		VccRx	+3.3 V Power Supply Receiver
11	LVC MOS-I/O	SCL	2-wire serial interface clock
12	LVC MOS-I/O	SDA	2-wire serial interface data
13		GND	Ground
14	CML-O	Rx3p	Receiver Non-Inverted Data Output
15	CML-O	Rx3n	Receiver Inverted Data Output
16		GND	Ground
17	CML-O	Rx1p	Receiver Non-Inverted Data Output
18	CML-O	Rx1n	Receiver Inverted Data Output
19		GND	Ground
20		GND	Ground
21	CML-O	Rx2n	Receiver Inverted Data Output
22	CML-O	Rx2p	Receiver Non-Inverted Data Output



23		GND	Ground
24	CML-O	Rx4n	Receiver Inverted Data Output
25	CML-O	Rx4p	Receiver Non-Inverted Data Output
26		GND	Ground
27	LVTTTL-O	ModPrsL	Module Present
28	LVTTTL-O	IntL	Interrupt
29		VccTx	+3.3V Power supply transmitter
30		Vcc1	+3.3V Power supply
31	LVTTTL-I	InitMode	Initialization mode
32		GND	Ground
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input
34	CML-I	Tx3n	Transmitter Inverted Data Input
35		GND	Ground
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input
37	CML-I	Tx1n	Transmitter Inverted Data Input
38		GND	Ground
39		GND	Ground
40	CML-I	Tx6n	Transmitter Inverted Data Input
41	CML-I	Tx6p	Transmitter Non-Inverted Data Output
42		GND	Ground
43	CML-I	Tx8n	Transmitter Inverted Data Input
44	CML-I	Tx8p	Transmitter Non-Inverted Data Output

45		GND	Ground
46		Reserved	
47		VS1	Module Vendor Specific 1
48		VccRx1	3.3V Power Supply
49		VS2	Module Vendor Specific 2
50		VS3	Module Vendor Specific 3
51		GND	Ground
52	CML-O	Rx7p	Receiver Non-Inverted Data Output
53	CML-O	Rx7n	Receiver Inverted Data Output
54		GND	Ground
55	CML-O	Rx5p	Receiver Non-Inverted Data Output
56	CML-O	Rx5n	Receiver Inverted Data Output
57		GND	Ground
58		GND	Ground
59	CML-O	Rx6n	Receiver Inverted Data Output
60	CML-O	Rx6p	Receiver Non-Inverted Data Output
61		GND	Ground
62	CML-O	Rx8n	Receiver Inverted Data Output
63	CML-O	Rx8p	Receiver Non-Inverted Data Output
64		GND	Ground
65		NC	No Connected

66		Reseved	
67		VccTx1	3.3V Power Supply
68		Vcc2	3.3V Power Supply
69		Reseved	
70		GND	Ground
71	CML-I	Tx7p	Transmitter Non-Inverted Data Output
72	CML-I	Tx7n	Transmitter Inverted Data Output
73		GND	Ground
74	CML-I	Tx5p	Transmitter Non-Inverted Data Output
75	CML-I	Tx5n	Transmitter Inverted Data Output
76		GND	Ground

## VII. Recommended QSFP-DD Host Board Schematic

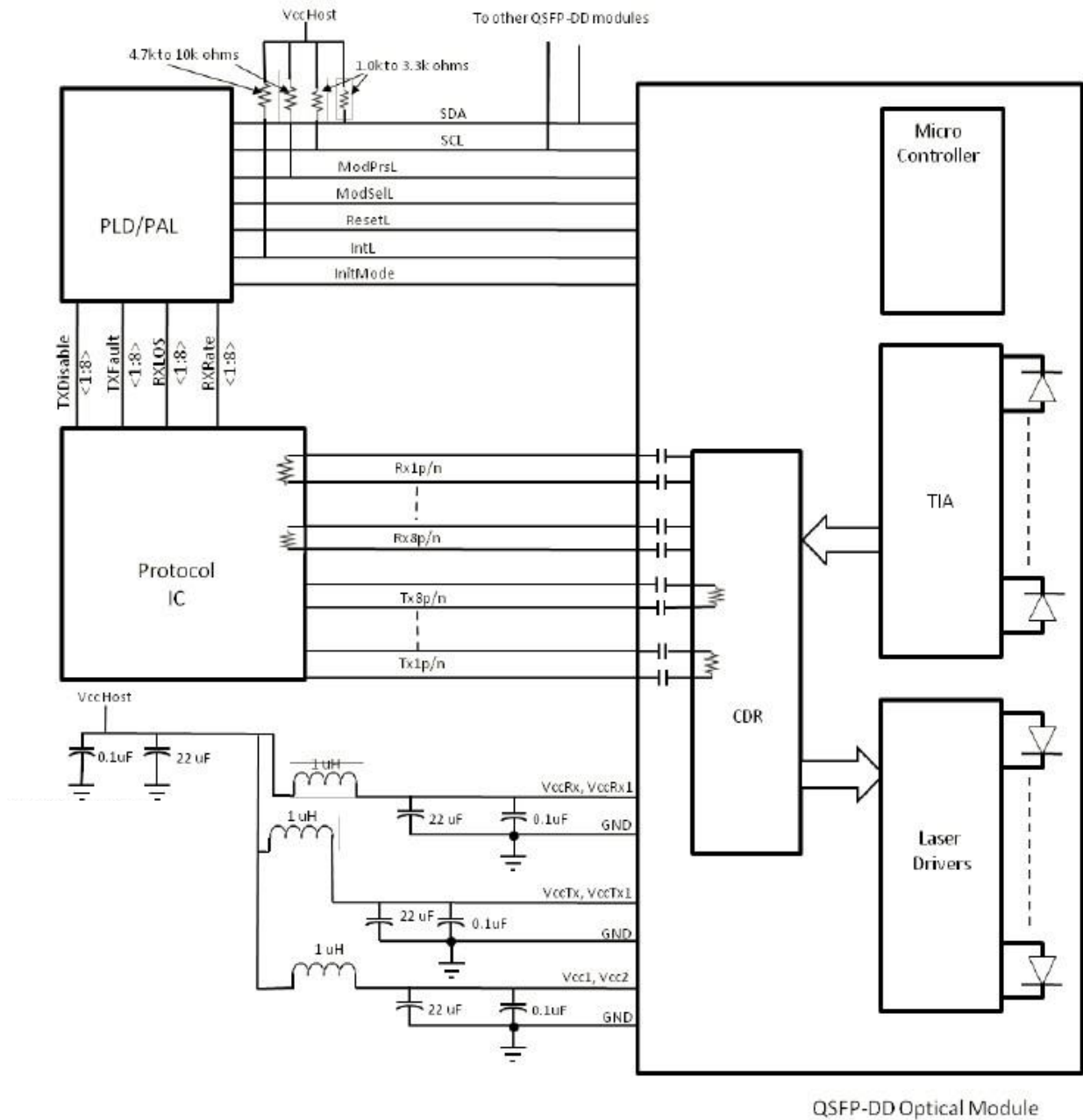


Figure 2 – Recommended QSFP-DD Host Board Schematic

### Notes:

1. Filter capacitor values are informative and vary depending on applications, 0.1  $\mu F$  capacitors should be placed in close proximity to power pins and may be duplicated for individual pins to provide additional high frequency filtering.
2.  $V_{cc1}$  and/or  $V_{cc2}$  may be connected to  $V_{ccTx}$ ,  $V_{ccTx1}$  or  $V_{ccRx}$ ,  $V_{ccRx1}$  provided the applicable derating of the maximum current limit is used.

**Table 3 - Timing for Soft Control and Status Functions**

Parameter	Symbol	Min	Max	Unit	Notes
<b>MgmtInit Duration</b>			2000	ms	
<b>ResetL Assert Time</b>	t_reset_init	10		μs	
<b>IntL Assert Time</b>	ton_IntL		200	ms	
<b>IntL Deassert Time</b>	toff_IntL		500	ms	
<b>Rx LOS Assert Time</b>	ton_los		100	ms	
<b>Tx Fault Assert Time</b>	ton_Txfault		200	ms	
<b>Flag Assert Time</b>	ton_flag		200	ms	
<b>Mask Assert Time</b>	ton_mask		100	ms	
<b>Mask Deassert Time</b>	toff_mask		100	ms	
<b>Application or Rate Select Change Time</b>	t_ratesel		N/A	ms	1

**Notes:**

1.This feature is not supported

**Table 4 - I/O Timing for Squelch and Disable**

Parameter	Symbol	Min	Max	Unit	Notes
<b>Rx Squelch Assert Time</b>	ton_Rxsq		15	ms	
<b>Rx Squelch Deassert Time</b>	toff_Rxsq		15	ms	
<b>Tx Squelch Assert Time</b>	ton_Txsq		400	ms	1
<b>Tx Squelch Deassert Time</b>	toff_Txsq		400	ms	1
<b>Tx Disable Assert Time</b>	ton_Txdis		100	ms	

<b>Tx Disable Deassert Time</b>	toff_Txdis		400	ms	
<b>Rx Output Disable Assert Time</b>	ton_Rxdis		100	ms	
<b>Rx Output Disable Deassert Time</b>	toff_Rxdis		100	ms	
<b>Squelch Disable Assert Time</b>	ton_sqdis		100	ms	
<b>Squelch Disable Deassert Time</b>	toff_sqdis		100	ms	

**Notes:**

- 1. Not implemented by default

**VIII. Mechanical Diagram**

