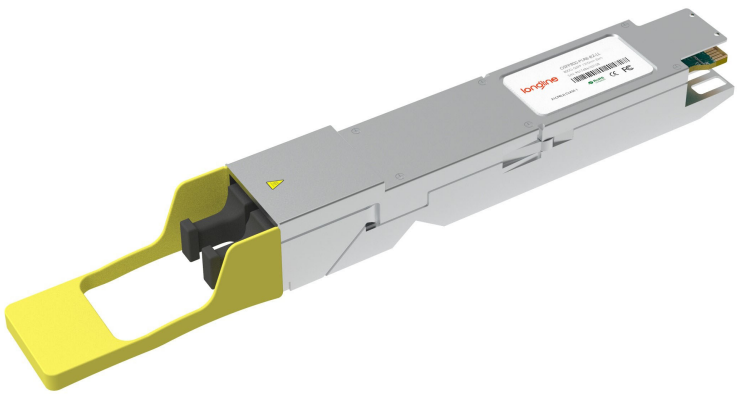
800GBASE-PLR8 OSFP 1310nm 10km Dual MTP/MPO-12 Transceiver

OSFP800-PLR8-B2-LL



Application

- 800G Ethernet
- Data Center
- Breakout 2x 400G PLR4
- Breakout 8x 100G LR

Features

- Maximum Power Consumption 16.5W
- 8x106.25 Gb/s PAM4 Modulation
- Single 3.3V Power Supply
- Operating Case Temperature Range: 0 to +70°C
- Two Wire Serial Interface with Digital Diagnostic Monitoring
- Class 1 Laser Safety

Standards

- Compliant with IEEE 802.3cu-2021
  -8x100GBASE-LR1 Optical Interface
- Compliant with IEEE P802.3ck D3.0
  -8x100GAUI-1 C2M Electrical Interface
- Compliant with OSFP MSA HW Rev 4.1
  -Type 2 Housing with Dual MPO-12 Connector
- Compliant with CMIS Rev 5.0

Description

Longline 's 800 GBASE -PLR 8 OSFP transceiver supports up to 10 km link lengths over single -mode fiber (SMF) via dual MTP /MPO -12 connectors. This transceiver is compliant with IEE802.3ck, IEEE 802.3cu and OSFP MSA standards. The built-in digital diagnostics monitoring (DDM) allows access to real-time operating parameters . It is suitable for Breakout 2x 400G PLR4 or 8x 100G LR, 800G Ethernet and Data Center Applications.

Products Specifications

I. Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	T_S	-40	85	ºC
Supply Voltage	V_{CC}	-0.5	3.6	V
Relative Humidity (Non-condensing)	RH	5	95	%
DataInput Voltage Differential	IV_{DIP}-$V_{DIN}I$		1	V
Control Input Voltage	V_I	-0.3	V_{CC}+0.5	V
Control Output Current	I_O	-20	20	mA

II. Recommended Operating Conditions

Parameter	Symbol	Min.	Typical	Max.	Unit
Operating Case Temperature	T_{OPR}	0		70	ºC
Power Supply Voltage	V_{CC}	3.135	3.3	3.465	V
Instantaneous Peak Current at Hot Plug	I_{CC_IP}			TBD	mA
Sustained Peak Current at Hot Plug	I_{CC_SP}			TBD	mA
Maximum Power Dissipation	P_D			16.5	W
Maximum Power Dissipation, Low Power Mode	P_{DLP}			2	W
Signalling Speed per Lane	DRL		53.125		GBd
Control Input Voltage High	V_{IH}	V_{CC}*0.7		V_{CC}+0.3	V
Control Input Voltage Low	V_{IL}	-0.3		V_{CC}*0.3	V
Two Wire Serial Interface Clock Rate				400	kHz
Power Supply Noise 1 kHz -1 MHz (p-p)				66	mVpp
Operating Distance		2		10000	m

III. Optical Characteristics

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Transmitter						
Wavelength	λ_C	1304.5	1311	1317.5	nm	
Side Mode Suppression Ratio	SMSR	30			dB	
Average Launch Power, each Lane	AOP_L	-1.9		4.8	dBm	1
Outer Optical Modulation Amplitude (OMAouter), each Lane for TDECQ<1.4dB for1.4dB<= TDECQ<=3.4dB	OMA_{outer}	1.1 –0.3+TDECQ		5	dBm	
Transmitter and Dispersion Eye Closure for PAM4 (TDECQ), each Lane	TDECQ			3.4	dB	
Transmitter Eye Closure for PAM4 (TECQ), each Lane	TECQ			3.4	dB	
|TDECQ-TECQ|				2.5	dB	
Over/Under-shoot				22	%	
Transmitter Power Excursion				2.8	dBm	
Average Launch Power of OFF Transmitter, each Lane	T_{OFF}			-15	dBm	
Extinction Ratio	ER	3.5			dB	
Transmitter Transition Time	Tr			17	ps	
$RIN_{15.6}OMA$	RIN			-136	dB/Hz	
Optical Return Loss Tolerance	ORL			15.6	dB	
Transmitter Reflectance	TR			-26	dB	2

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Receiver						
Wavelength	λ_{C0}	1304.5	1311	1317.5	nm	
Damage Threshold, each Lane	AOP_D	5.8			dBm	
Average Receive Power, each Lane	AOP_R	-8.2		4.8	dBm	
Receive Power (OMAouter), each Lane	OMA_R			5	dBm	
Receiver Reflectance	RR			-26	dB	
Receiver Sensitivity (OMAouter) for TECQ<1.4 dB for 1.4dB<=TECQ<=3.4dB	S_{OMA}			–6.1 –7.5+TECQ	dBm	3
Stressed Receiver Sensitivity (OMAouter), each Lane	SRS			-4.1	dBm	4
Conditions of Stressed Receiver Sensitivity Test						
Stressed Eye Closure for PAM4 (SECQ), Lane Under Test	SECQ		3.4		dB	

NOTE 1: Average launch power, each lane (min) is informative and not the principal indicator of signal strength.

NOTE 2: Transmitter reflectance is defined looking into the transmitter.

NOTE 3: Receiver sensitivity (OMAouter), each lane (max) is informative and is defined for a transmitter with a value of SECQ up to 3.4 dB.

NOTE 4: Measured with conformance test signal at TP3 for the BER = $2.4x10^{-4}$.

IV. Electrical Characteristics

1. Electrical Specification High Speed Signal (Compliant with IEEE802.3ck C2M)

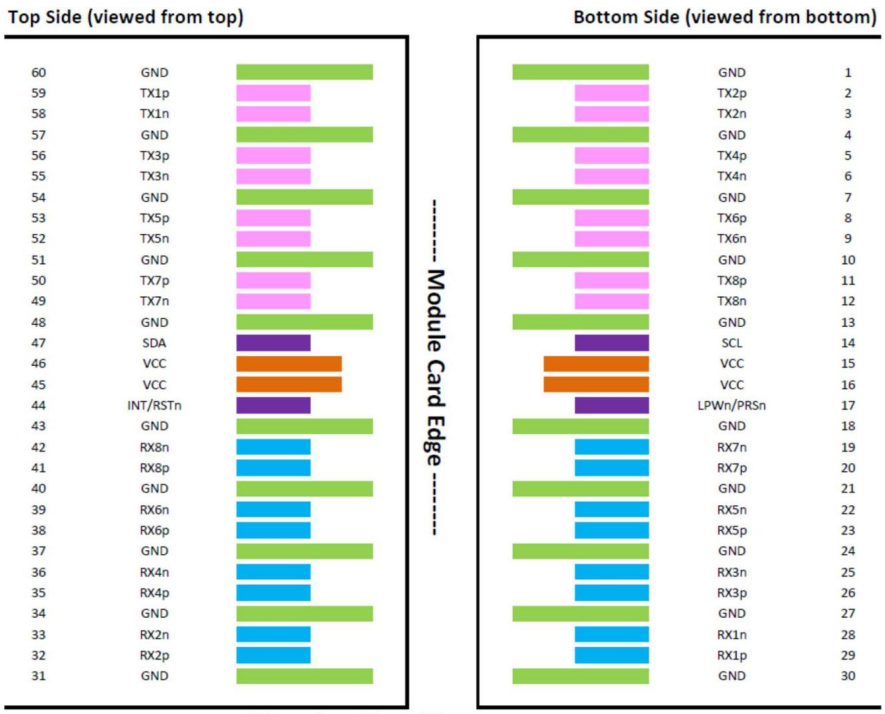
Parameter	Symbol	Min.	Typical	Max.	Unit
Receiver (Module Output, TP4)					
AC Common-mode Output Voltage (RMS)				25	mV
Differential Peak-to-peak Output Voltage — **Short Mode**				600	mV
Differential Peak-to-peak Output Voltage — **Long Mode**				845	mV
Eye Height	EH	15			mV
Vertical Eye Closure	VEC			12	dB
Common-mode to Differential-mode Return Loss	RLD_C		802.3ck 120G-1		dB
Effective Return Loss	ERL	8.5			dB
Differential Termination Mismatch				10	%
Transition Time		8.5			ps
DC Common-mode Voltage Tolerance		-0.35		2.85	V
Transmitter (Module Input, TP1)					
Differential Pk-pk Input Voltage Tolerance (TP1a)		750			mV
AC Common-mode RMS Voltage Tolerance (TP1a)		25			mV
Differential-mode to Common-mode Return Loss	RL_{cd}		802.3ck 120G-2		dB
Effective Return Loss	ERL	8.5			dB

Parameter	Symbol	Min.	Typical	Max.	Unit
Differential Termination Mismatch				10	%
Single-ended Voltage Tolerance Range		-0.4		3.3	V
DC Common-mode Voltage Tolerance		-0.35		2.85	V

2. Electrical Specification Low Speed Control and Sense Signals(Compliant with QSFP-DD HW Rev6.01 Table 14)

Parameter	Symbol	Min.	Max.	Unit
Module Output SCL and SDA	V_{OL}	0	0.4	V
Module Input SCL and SDA	V_{IL}	-0.3	V_{CC}*0.3	V
	V_{IH}	V_{CC}*0.7	V_{CC}+0.5	V
InitMode, ResetL and ModSelL	V_{IL}	-0.3	0.8	V
	V_{IH}	2	V_{CC}+0.3	V
IntL	V_{OL}	0	0.4	V
	V_{OH}	V_{CC}-0.5	V_{CC}+0.3	V

V. Pin Description



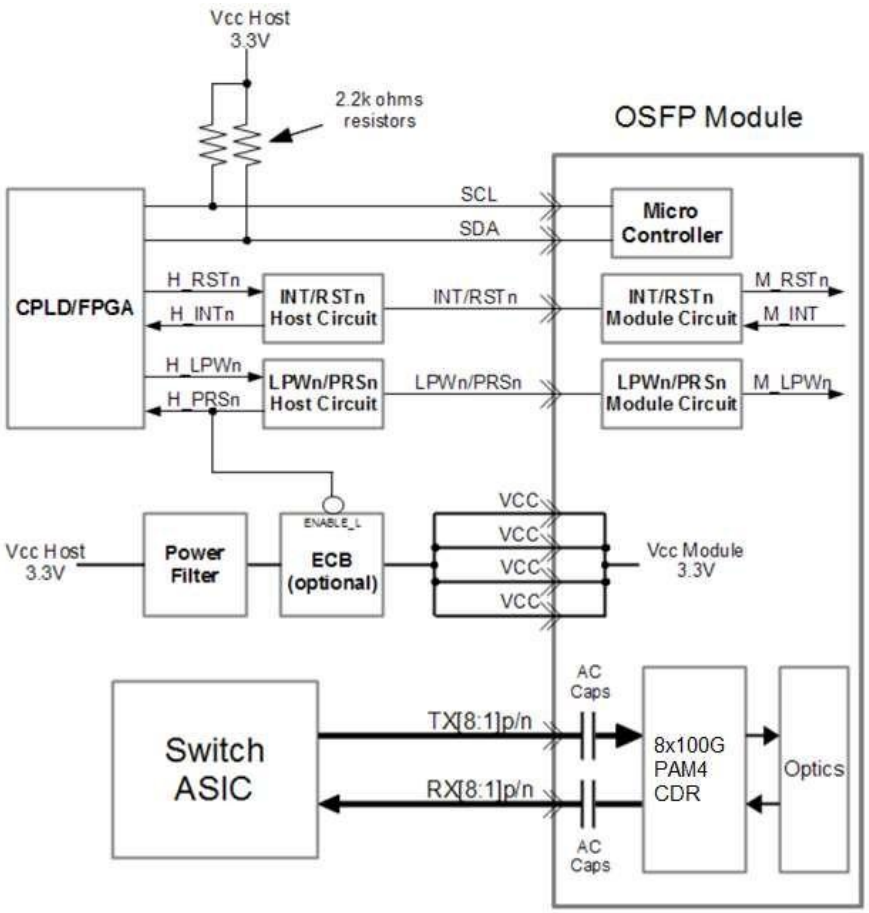
Pin	Symbol	Description	Logic
1	GND	Ground	
2	TX2p	Transmitter Data Non-Inverted	CML-I
3	TX2n	Transmitter Data Inverted	CML-I
4	GND	Ground	
5	TX4p	Transmitter Data Non-Inverted	CML-I
6	TX4n	Transmitter Data Inverted	CML-I
7	GND	Ground	
8	TX6p	Transmitter Data Non-Inverted	CML-I
9	TX6n	Transmitter Data Inverted	CML-I

Pin	Symbol	Description	Logic
10	GND	Ground	
11	TX8p	Transmitter Data Non-Inverted	CML-I
12	TX8n	Transmitter Data Inverted	CML-I
13	GND	Ground	
14	SCL	2-wire Serial Interface Clock	LVCMOS-I/O
15	V_{CC}	+3.3V Power	
16	V_{CC}	+3.3V Power	
17	LPWn/PRSn	Low-Power Mode/Module Present	Multi-Level
18	GND	Ground	
19	RX7n	Receiver Data Inverted	CML-O
20	RX7p	Transmitter Data Non-Inverted	CML-O
21	GND	Ground	
22	RX5n	Receiver Data Inverted	CML-O
23	RX5p	Receiver Data Non-Inverted	CML-O
24	GND	Ground	
25	RX3n	Receiver Data Inverted	CML-O
26	RX3p	Receiver Data Non-Inverted	CML-O
27	GND	Ground	

Pin	Symbol	Description	Logic
28	RX1n	Receiver Data Inverted	CML-O
29	RX1p	Receiver Data Non-Inverted	CML-O
30	GND	Ground	
31	GND	Ground	
32	RX2p	Receiver Data Non-Inverted	CML-O
33	RX2n	Receiver Data Inverted	CML-O
34	GND	Ground	
35	RX4p	Receiver Data Non-Inverted	CML-O
36	RX4n	Receiver Data Inverted	CML-O
37	GND	Ground	
38	RX6p	Receiver Data Non-Inverted	CML-O
39	RX6n	Receiver Data Inverted	CML-O
40	GND	Ground	
41	RX8p	Receiver Data Non-Inverted	CML-O
42	RX8n	Receiver Data Inverted	CML-O
43	GND	Ground	
44	INT/RSTn	Module Interrupt/Module Reset	Multi-Level
45	V_{CC}	3.3V Power	

Pin	Symbol	Description	Logic
46	V_{CC}	3.3VPower	
47	SDA	2-wire Serial Interface Data	LVCMOS-I/O
48	GND	Ground	
49	TX7n	Transmitter Data Inverted	CML-I
50	TX7p	Transmitter Data Non-Inverted	CML-I
51	GND	Ground	
52	TX5n	Transmitter Data Inverted	CML-I
53	TX5p	Transmitter Data Non-Inverted	CML-I
54	GND	Ground	
55	TX3n	Transmitter Data Inverted	CML-I
56	TX3p	Transmitter Data Non-Inverted	CML-I
57	GND	Ground	
58	TX1n	Transmitter Data Inverted	CML-I
59	TX1p	Transmitter Data Non-Inverted	CML-I
60	GND	Ground	

VI. Recommended OSFP Host Board Schematic



VII. Digital Diagnostic Functions

Parameter	Range	Accuracy	Unit	Calibration
Temperature	0 to 70	±3	°C	Internal
Voltage	0 to V_{CC}	0.1	V	Internal
Tx Bias Current (each Lane)	0 to 100	10%	mA	Internal
Tx Output Power (each Lane)	-1.9 to +4.8	±3	dB	Internal
Rx Receive Power (each Lane)	-8.2 to +4.8	±3	dB	Internal

VIII. Diagram Mechanial Drawing