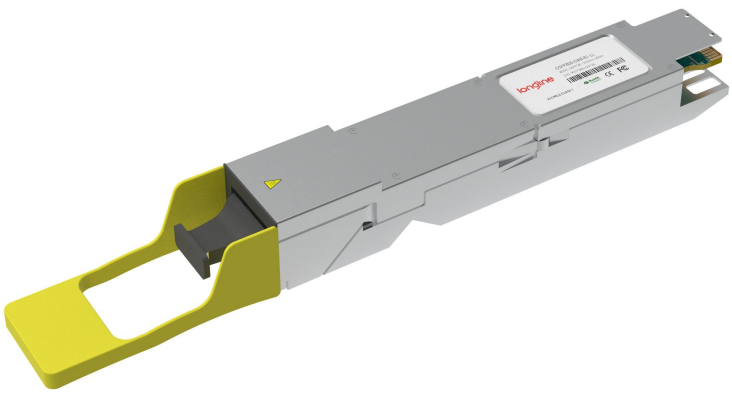
800GBASE-DR8 OSFP 1310nm 500m MTP/MPO-16 SMF Transceiver

OSFP800-DR8-B1-LL



Application

- 800G Ethernet
- Data Center

Standards

- Compliant with IEEE 802.3cu-2021
  -8x100GBASE-DR Optical Interface
- Compliant with IEEE P802.3ck D3.0
  -8x100GAUI-1 C2M Electrical Interface
- Compliant with OSFP MSA HW Rev 4.1
  -Type 2 housing with MPO-16 Connector
- Compliant with CMIS Rev 5.0

Features

- Maximum Power Consumption: 16.5W
- Case Operating Temperature 0℃ to 70℃
- Two Wire Serial Interface with Digital Diagnostic Monitoring
- Complies with EU Directive 2011/65/EU
- Class 1 Laser Safety

Description

The 800GBASE-DR8 OSFP transceiver is designed for 800GBASE Ethernet throughput up to 500m over singlemode fiber (SMF) with MPO-16 connectors. This transceiver is compliant with IEEE P802.3ck, IEEE 802.3cu, OSFP MSA. The built-in digital diagnostics monitoring (DDM) allows access to real-time operating parameters.

It is suitable for 800G Ethernet, Data Center, Breakout 2x 400G DR4 or 8x 100G DR Application.

Product Specifications

I. Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	T_S	-40	85	ºC
Supply Voltage	V_{CC}	-0.5	3.6	V
Relative Humidity (Non-condensing)	RH	5	95	%
Data Input Voltage Differential	IV_{DIP}-$V_{DIN}I$		1	V
Control Input Voltage	V_I	-0.3	V_{CC}+0.5	V
Control Output Current	I_O	-20	20	mA

II. Recommended Operating Environment

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Operating Case Temperature	T_{OPR}	0		70	ºC	1
Power Supply Voltage	V_{CC}	3.135	3.3	3.465	V	
Instantaneous Peak Current at Hot Plug	I_{CC_IP}			TBD	mA	
Sustained Peak Current at Hot Plug	I_{CC_SP}			TBD	mA	
Maximum Power Dissipation	P_D			16.5	W	

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Maximum Power Dissipation, Low Power Mode	P_{DLP}			2	W	
Signalling Speed per Lane	DRL		53.125		GBd	
Control Input Voltage High	V_{IH}	V_{CC}*0.7		V_{CC}+0.3	V	
Control Input Voltage Low	V_{IL}	-0.3		V_{CC}*0.3	V	
Two Wire Serial Interface Clock Rate				400	kHz	
Power Supply Noise 1 kHz -1 MHz (p-p)				66	mVpp	
Operating Distance		2		500	m	

III. Optical Characteristics

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Transmitter						
Wavelength	λ_C	1304.5	1311	1317.5	nm	
Side Mode Suppression Ratio	SMSR	30			dB	
Average Launch Power, each Lane	AOP_L	-2.9		4.0	dBm	1
Outer Optical Modulation Amplitude (OMA_{outer}), each Lane	T_{OMA}	-0.8		4.2	dBm	
Launch power in OMAouter minus TDECQ, each Lane for extinction ratio >= 5 dB for extinction ratio < 5 dB	$T_{OMA-TDECQ}$	-2.2 -1.9			dBm	
Transmitter and Dispersion Eye Closure for PAM4 (TDECQ), each Lane	TDECQ			3.4	dB	
TDECQ – 10log10(Ceq), each Lane	Ceq			3.4	dB	
Average Launch Power of OFF Transmitter, each Lane	T_{OFF}			-15	dBm	

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Extinction Ratio	ER	3.5			dB	
Transmitter Transition Time	Tr			17	ps	
$RIN_{15.5}OMA$	RIN			-136	dB/Hz	
Optical Return Loss Tolerance	ORL			15.5	dB	
Transmitter Reflectance	T_R			-26	dB	2
Receiver						
Wavelength	λ_{C0}	1304.5	1311	1317.5	nm	
Damage Threshold, each Lane	AOP_D	5			dBm	
Average Receive Power, each Lane	AOP_R	-5.9		4	dBm	
Receive Power (OMAouter), each Lane	OMA_R			4.2	dBm	
Receiver Reflectance	RR			-26	dB	
Receiver Sensitivity (OMAouter), each Lane	SOMA			Max(-3.9, SECQ -5.3	dBm	3
Stressed Receiver Sensitivity (OMAouter), each Lane	SRS			-1.9	dBm	4
Conditions of Stressed Receiver Sensitivity Test						
Stressed Eye Closure for PAM4 (SECQ), Lane Under Test	SECQ		3.4		dB	
SECQ – 10log10(Ceq), Lane Under Test	Ceq			3.4	dB	

Notes:

1. Average launch power, each lane (min) is informative and not the principal indicator of signal strength

2. Transmitter reflectance is defined looking into the transmitter.

3 Receiver sensitivity (OMAouter), each lane (max) is informative and is defined for a transmitter with a value of SECQ up to 3.4 dB.

4. Measured with conformance test signal at TP3 for the BER = $2.4x10^{-4}$.

IV. Electrical Characteristics

1. Electrical Specification High Speed Signal (Compliant with IEEE802.3ck C2M)

Parameter	Symbol	Min.	Typical	Max.	Unit
Receiver (Module Output, TP4)					
AC Common-mode Output Voltage (RMS)				25	mV
Differential peak-to-peak Output Voltage **Short Mode** **Long Mode**				600 845	mV
Eye Height	EH	15			mV
Vertical Eye Closure	VEC			12	dB
Common-mode to Differential-mode Return Loss	RLDc		802.3ck 120G-1		dB
Effective Return Loss	ERL	8.5			dB
Differential Termination Mismatch				10	%
Transition Time		8.5			ps
DC Common-mode Voltage Tolerance		-0.35		2.85	V
Transmitter (Module Input, TP1)					
Differential pk-pk Input Voltage Tolerance (TP1a)		750			mV
AC Common-mode RMS Voltage Tolerance (TP1a)		25			mV
Differential-mode to Common-mode Return Loss	RLcd		802.3ck 120G-2		dB
Effective Return Loss	ERL	8.5			dB
Differential Termination Mismatch				10	%
Single-ended Voltage Tolerance Range		-0.4		3.3	V
DC Common-mode Voltage Tolerance		-0.35		2.85	V

2. Electrical Specification Low Speed Control and Sense Signals (Compliant with QSFP-DD HW Rev 6.01)

Parameter	Symbol	Min.	Max.	Unit
Module Output SCL and SDA	V_{OL}	0	0.4	V
Module Input SCL and SDA	V_{IL}	-0.3	V_{CC}*0.3	V
	V_{IH}	V_{CC}*0.7	V_{CC}+0.5	V
InitMode, ResetL and ModSelL	V_{IL}	-0.3	0.8	V
	V_{IH}	2	V_{CC}+0.3	V
IntL	V_{OL}	0	0.4	V
	V_{OH}	V_{CC}-0.5	V_{CC}+0.3	V

V. Pin Description

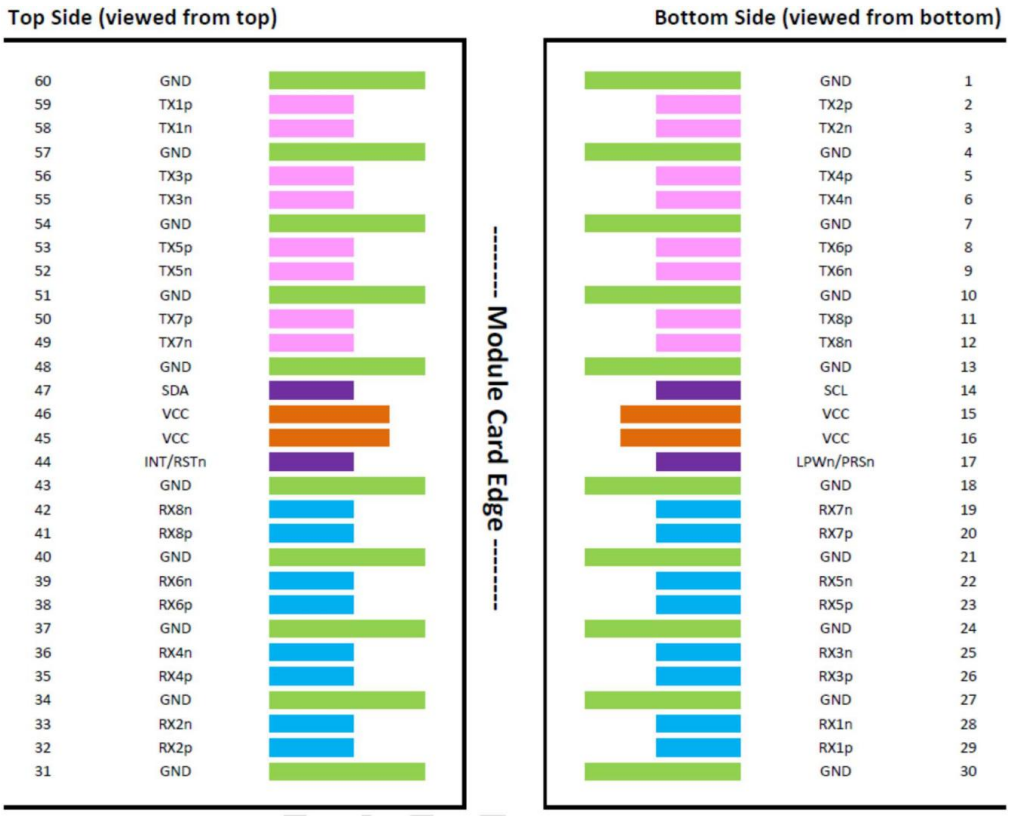


Figure 1 – Pinout definitions of OSFP module inputs/outputs

Pin#	Symbol	Description	Logic	Pin#	Symbol	Description	Logic
1	GND	Ground		31	GND	Ground	
2	TX2p	Transmitter Data Non-Inverted	CML-I	32	RX2p	Receiver Data Non-Inverted	CML-O
3	TX2n	Transmitter Data Inverted	CML-I	33	RX2n	Receiver Data Inverted	CML-O
4	GND	Ground		34	GND	Ground	
5	TX4p	Transmitter Data Non-Inverted	CML-I	35	RX4p	Receiver Data Non-Inverted	CML-O
6	TX4n	Transmitter Data Inverted	CML-I	36	RX4n	Receiver Data Inverted	CML-O
7	GND	Ground		37	GND	Ground	
8	TX6p	Transmitter Data Non-Inverted	CML-I	38	RX6p	Receiver Data Non-Inverted	CML-O
9	TX6n	Transmitter Data Inverted	CML-I	39	RX6n	Receiver Data Inverted	CML-O
10	GND	Ground		40	GND	Ground	
11	TX8p	Transmitter Data Non-Inverted	CML-I	41	RX8p	Receiver Data Non-Inverted	CML-O
12	TX8n	Transmitter Data Inverted	CML-I	42	RX8n	Receiver Data Inverted	CML-O
13	GND	Ground		43	GND	Ground	
14	SCL	2-wire Serial Interface Clock	LVCMOS-I/O	44	INT/RSTn	Module Interrupt/Module Reset	Multi-Level
15	V_{CC}	3.3V Power		45	V_{CC}	3.3V Power	
16	V_{CC}	3.3V Power		46	V_{CC}	3.3V Power	
17	LPWn/PRSn	Low-Power Mode/Module Present	Multi-Level	47	SDA	2-wire Serial Interface Data	LVCMOS-I/O
18	GND	Ground		48	GND	Ground	

Pin#	Symbol	Description	Logic	Pin#	Symbol	Description	Logic
19	RX7n	Receiver Data Inverted	CML-O	**49**	TX7n	Transmitter Data Inverted	CML-I
20	RX7p	Receiver Data Non-Inverted	CML-O	**50**	TX7p	Transmitter Data Non-Inverted	CML-I
21	GND	Ground		**51**	GND	Ground	
22	RX5n	Receiver Data Inverted	CML-O	**52**	TX5n	Transmitter Data Inverted	CML-I
23	RX5p	Receiver Data Non-Inverted	CML-O	**53**	TX5p	Transmitter Data Non-Inverted	CML-I
24	GND	Ground		**54**	GND	Ground	
25	RX3n	Receiver Data Inverted	CML-O	**55**	TX3n	Transmitter Data Inverted	CML-I
26	RX3p	Receiver Data Non-Inverted	CML-O	**56**	TX3p	Transmitter Data Non-Inverted	CML-I
27	GND	Ground		**57**	GND	Ground	
28	RX1n	Receiver Data Inverted	CML-O	**58**	TX1n	Transmitter Data Inverted	CML-I
29	RX1p	Receiver Data Non-Inverted	CML-O	**59**	TX1p	Transmitter Data Non-Inverted	CML-I
30	GND	Ground		**60**	GND	Ground	

VI. Digital Diagnostic Functions

Parameter	Range	Accuracy	Unit	Calibration
Temperature	0~70	±3	ºC	Internal
Voltage	0~V_{CC}	0.1	V	Internal
Tx Bias Current (each Lane)	0~100	10%	mA	Internal
Tx Output Power (each Lane)	-2.9~4	±3	dB	Internal
Rx Receive Power (each Lane)	-5.9~4	±3	dB	Internal

VII. Recommended OSFP Host Board Schematic

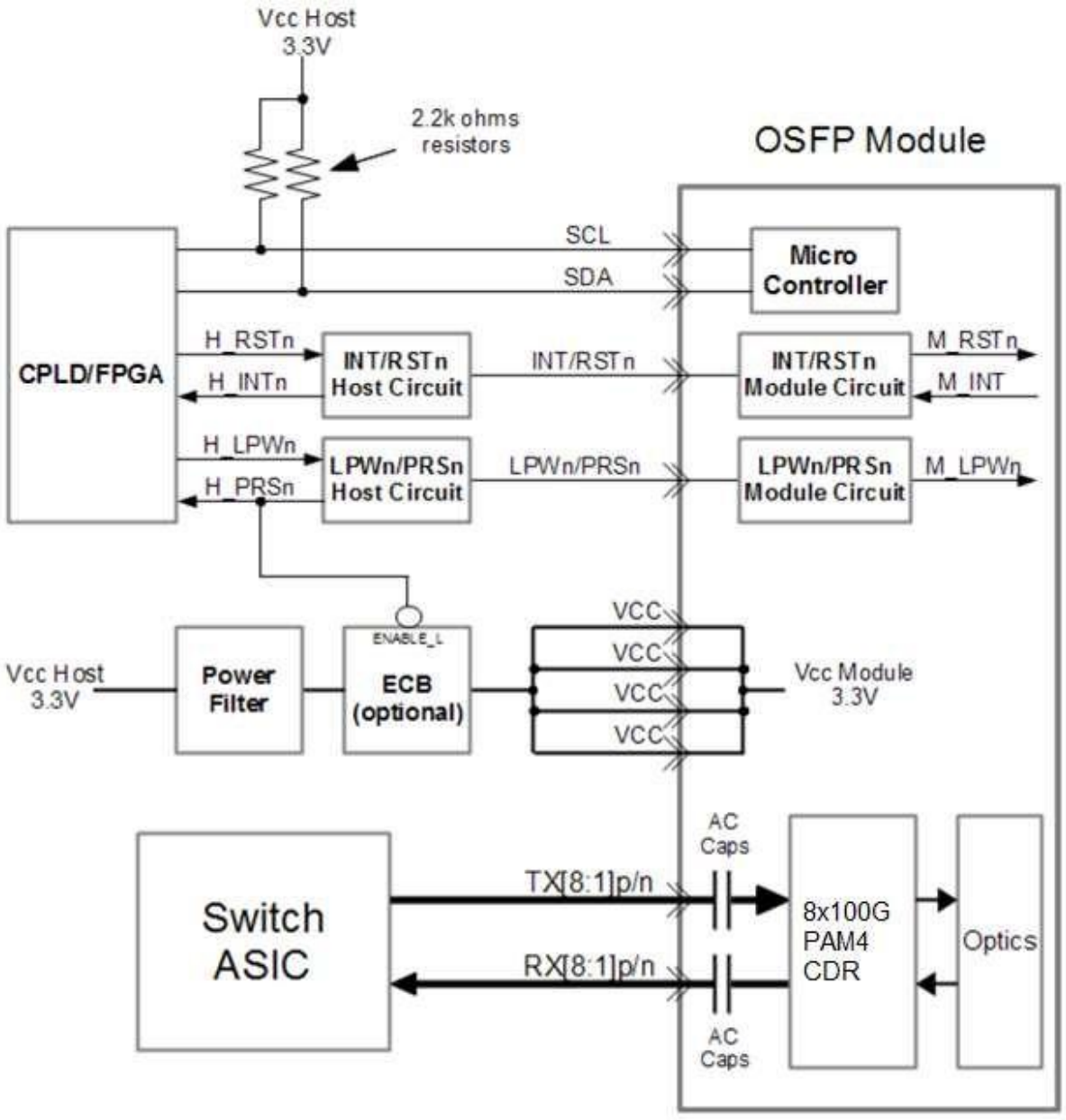


Figure 2 – Recommended OSFP Host Board Schematic

VIII. Mechanical Diagram