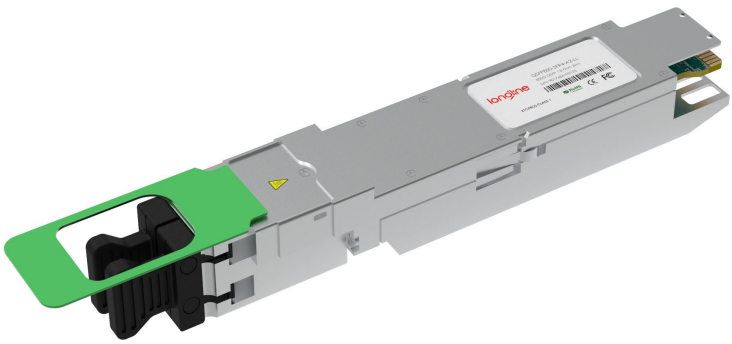
OSFP 800GBASE-2FR4 1310nm 2km Transceiver

OSFP800-2FR4-A2-LL



Application

- 800G Ethernet
- 2x 400GBASE-FR4
- Data Center
- Cloud Networks

Features

- Compliant with IEEE 802.3cu-2021 2x400GBASE-FR4 Optical Interface
- Compliant with IEEE P802.3ck D2.2 2x400GAUI-4 C2M Electrical Interface
- Compliant with QSFP-DD CMIS Rev 5.0
- Dual LC Connector
- Single +3.6V Power Supply
- DDM Function Implemented
- Hot-pluggable OSFP Form Factor
- Up to 2km Transmission on Single Mode Fiber
- Maximum Power Consumption 16w
- Class 1 Laser Safety
- Operating Temperature Range: 0℃ ~ +70 ℃

Description

The 800GBASE-2FR4 OSFP Optical Transceiver Module is designed for 800GBASE Ethernet throughput up to 2km over single-mode fiber (SMF) with duplex LC connectors. The 800 Gigabit Ethernet signal is carried over four wavelengths at 1271, 1291, 1311, 1331 nm. This transceiver is compliant with IEE802.3ck, IEEE 802.3cu, OSFP MSA. The built-in digital diagnostics monitoring (DDM) allows access to real-time operating parameters. It is suitable for 800G Ethernet, Breakout 2x 400G FR4, Data Center, Cloud Networks.

Product Specifications

I. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Storage Temperature Range	TS	-40	85	ºC
Supply Voltage	VCC	-0.5	3.6	V
Relative Humidity (non-condensing)	RH	5	95	%
Data Input Voltage Differential	IVDIP-VDINI		1	V
Control Input Voltage	VI	-0.3	VCC+0.5	V
Control Output Current	IO	-20	20	mA

II. Recommended Operating Conditions

Parameter	Symbol	Min	Typ.	Max	Unit	Notes
Operating Case Temperature	TOPR	0		70	ºC	
Power Supply Voltage	VCC	3.135	3.3	3.465	V	
Instantaneous peak current at hot plug	ICC_IP				mA	
Sustained peak current at hot plug	ICC_SP				mA	
Maximum Power Dissipation	PD			16	W	

Maximum Power Dissipation, Low Power Mode	PDLP				W	
Signalling Speed per Lane	DRL		53.125		GBd	
Control Input Voltage High	VIH	VCC*0.7		VCC+0.3	V	
Control Input Voltage Low	VIL	-0.3		VCC*0.3	V	
Two Wire Serial Interface Clock Rate				400	kHz	
Power Supply Noise 1 kHz - 1 MHz (p-p)				66	mVpp	
Operating Distance		2		2000	m	

III. Optical Characteristics

Parameter	Symbol	Min	Typ.	Max	Unit	Notes
Wavelength Assignment	**L0**	1264.5	1271	1277.5	nm	
	L1	1284.5	1291	1297.5	nm	
	L2	1304.5	1311	1317.5	nm	
	L3	1324.5	1331	1337.5	nm	
Transmitter (per Lane)						
Side Mode Suppression Ratio	SMSR	30			dB	
Total average launch power (max)	AOPT			10.4		
Average Launch Power, each lane	AOPL	-3.2		4.4	dBm	1
Outer Optical Modulation Amplitude (OMAouter), each Lane for TDECQ <1.4 dB for 1.4 dB ≤TDECQ ≤3.4 dB	TOMA	-0.2 –1.6 + TDECQ		3.7	dBm	
Difference in launch power between any two lanes (OMAouter) (max)	AOPd			3.9	dB	
Transmitter and Dispersion Eye Closure for PAM4 (TDECQ), each lane	TDECQ			3.4	dB	

| TDECQ – TECQ |				2.5	dB	
Over/under-shoot				22	%	
Transmitter power excursion				1.8	dBm	
Average Launch Power of OFF Transmitter, each lane	TOFF			-16	dBm	
Extinction Ratio	ER	3.5			dB	
Transmitter transition time (max)	Tr			17	ps	
RIN17.1OMA (max)	RIN			-136	dB/Hz	
Optical Return Loss Tolerance	ORL			17.1	dB	
Transmitter Reflectance	TR			-26	dB	2
Receiver (Per lane)						
Damage Threshold, each Lane	AOPD	5.4			dBm	
Average Receive Power, each Lane	AOPR	-7.2		4.4	dBm	
Receive Power (OMAouter), each Lane	OMAR			3.7	dBm	
Difference in receive power between any two lanes (OMAouter) (max)	AOPg			4.1		
Receiver Reflectance	RR			-26	dB	
Receiver sensitivity (OMAouter), each lane for TECQ < 1.4 dB for 1.4 dB≤ TECQ ≤3.4 dB	SOMA			-4.6 –6 + TECQ	dBm	
Stressed Receiver Sensitivity (OMAouter), each Lane	SRS			-2.6	dBm	3
Conditions of stressed receiver sensitivity test:						
Stressed eye closure for PAM4 (SECQ), lane under test			3.4		dB	
OMAouter of each aggressor lane			1.4		dBm	

Notes:
1: Average launch power, each lane (min) is informative and not the principal indicator of signal strength
2: Transmitter reflectance is defined looking into the transmitter
3./Measured with conformance test signal at TP3 for the BER = 2.4x10-4

IV. Electrical Characteristics(compliant with IEEE P802.3ck C2M))

Parameter	Symbol	Min	Typ.	Max	Unit	Notes
Transmitter (per Lane)						
Differential pk-pk input Voltage tolerance (TP1a)		900			mV	
AC common-mode RMS voltage tolerance (TP1a)		25			mV	
Differential to common-mode return loss	RLcd	802.3ck 120G-2			dB	
Effective return loss, ERL	ERL	8.5			dB	
Differential termination mismatch				10	%	
Single-ended voltage tolerance range		-0.4		3.3	V	
DC common-mode voltage tolerance		-0.35		2.85	V	
Receiver (per Lane)						
AC common-mode output Voltage (RMS)				25	mV	
Differential peak-to-peak output voltage ShortmodeLongmode				600900	mV mV	
Eye height, differential	EH	15			mV	
Vertical eye closure	VEC			12	dB	
Common-mode to differential return loss	RLDc	802.3ck 120G-1			dB	
Effective return loss, ERL	ERL	8.5			dB	
Differential termination mismatch				10	%	
Transition time (20% to 80%)		8.5			ps	
DC common-mode voltage		-350		2850	mV	

V. Principle Diagram

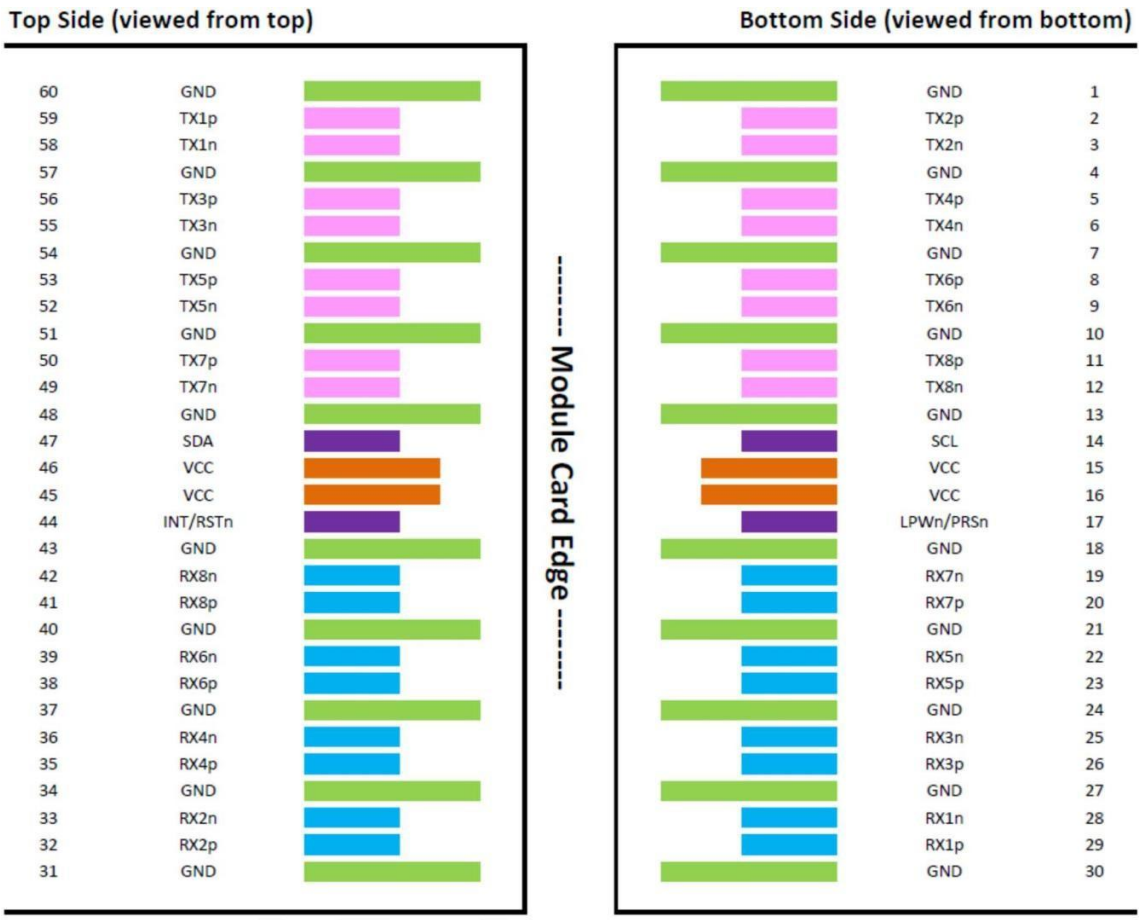


Figure 1. Pinout definitions of OSFP module inputs/outputs

VI. Pin Description

PIN	Symbol	Description	Logic	Note
1	GND	Ground		
2	TX2p	Transmitter Data Non-Inverted	CML-I	
3	TX2n	Transmitter Data Inverted	CML-I	
4	GND	Ground		
5	TX4p	Transmitter Data Non-Inverted	CML-I	
6	TX4n	Transmitter Data Inverted	CML-I	
7	GND	Ground		
8	TX6p	Transmitter Data Non-Inverted	CML-I	
9	TX6n	Transmitter Data Inverted	CML-I	
10	GND	Ground		
11	TX8p	Transmitter Data Non-Inverted	CML-I	
12	TX8n	Transmitter Data Inverted	CML-I	
13	GND	Ground		
14	SCL	2-wire Serial interface clock	LVCMOS-I/O	
15	VCC	+3.3V Power		
16	VCC	+3.3V Power		
17	LPWn/P RSn	Low-Power Mode / Module Present	Multi-Level	
18	GND	Ground		
19	RX7n	Receiver Data Inverted	CML-O	
20	RX7p	Receiver Data Non-Inverted	CML-O	
21	GND	Ground		

22	RX5n	Receiver Data Inverted	CML-O	
23	RX5p	Receiver Data Non-Inverted	CML-O	
24	GND	Ground		
25	RX3n	Receiver Data Inverted	CML-O	
26	RX3p	Receiver Data Non-Inverted	CML-O	
27	GND	Ground		
28	RX1n	Receiver Data Inverted	CML-O	
29	RX1p	Receiver Data Non-Inverted	CML-O	
30	GND	Ground		
31	GND	Ground		
32	RX2p	Receiver Data Non-Inverted	CML-O	
33	RX2n	Receiver Data Inverted	CML-O	
34	GND	Ground		
35	RX4p	Receiver Data Non-Inverted	CML-O	
36	RX4n	Receiver Data Inverted	CML-O	
37	GND	Ground		
38	RX6p	Receiver Data Non-Inverted	CML-O	
39	RX6n	Receiver Data Inverted	CML-O	
40	GND	Ground		
41	RX8p	Receiver Data Non-Inverted	CML-O	
42	RX8n	Receiver Data Inverted	CML-O	
43	GND	Ground		
44	INT/RSTn	Module Interrupt / Module Reset	Multi- Level	
45	VCC	+3.3V Power		
46	VCC	+3.3V Power		
47	SDA	2-wire Serial interface data	LVCM OS-I/O	
48	GND	Ground		
49	TX7n	Transmitter Data Inverted	CML-I	
50	TX7p	Transmitter Data Non-Inverted	CML-I	
51	GND	Ground		
52	TX5n	Transmitter Data Inverted	CML-I	
53	TX5p	Transmitter Data Non-Inverted	CML-I	
54	GND	Ground		

55	TX3n	Transmitter Data Inverted	CML-I	
56	TX3p	Transmitter Data Non-Inverted	CML-I	
57	GND	Ground		
58	TX1n	Transmitter Data Inverted	CML-I	
59	TX1p	Transmitter Data Non-Inverted	CML-I	
60	GND	Ground		

VII. Recommended OSFP Host Board Schematic

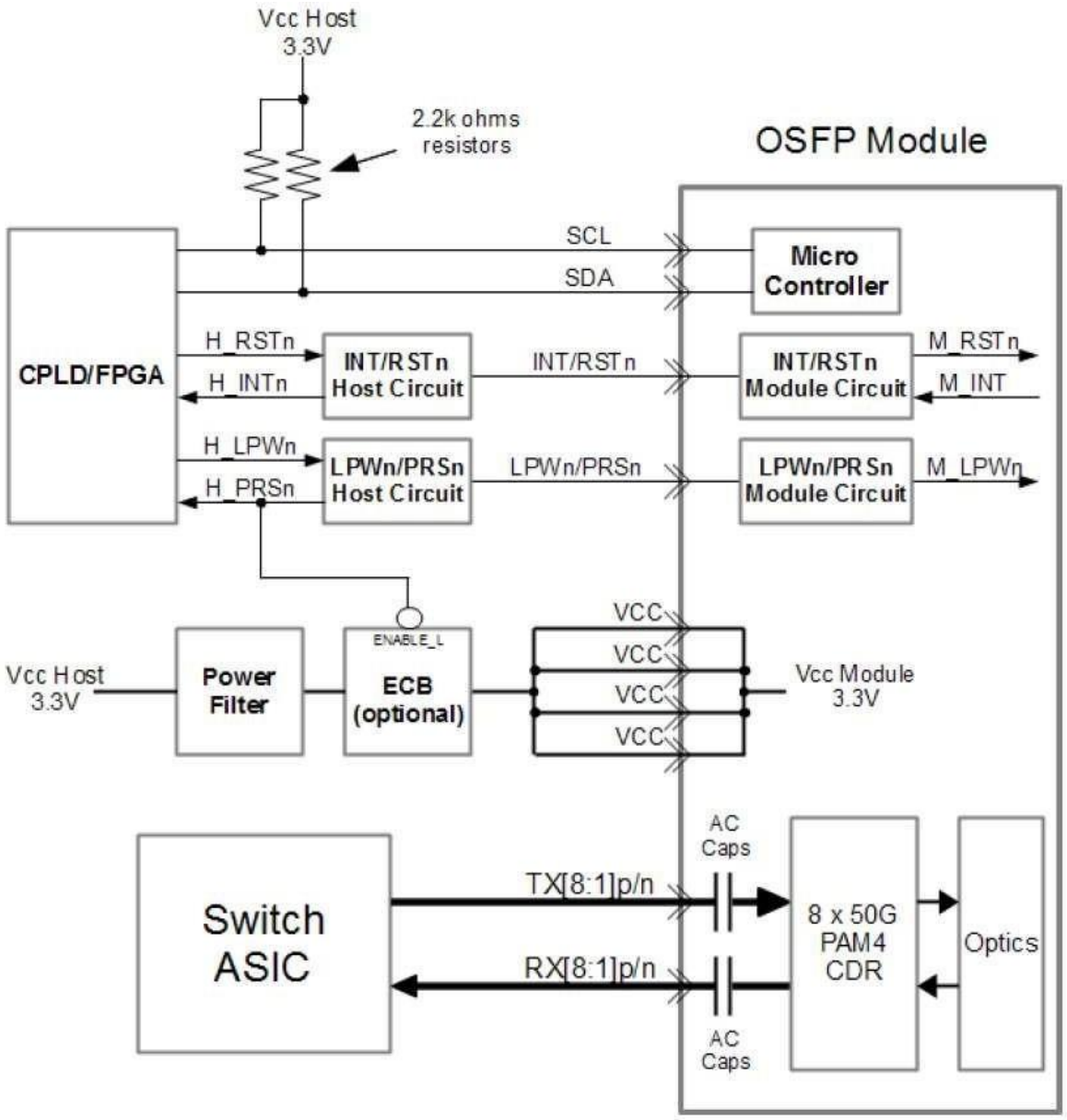


Figure 2. Recommended OSFP Host Board Schematic

VIII. Digital Diagnostics

Parameter	Range	Accuracy	Unit	Calibration
Temperature	0 to 70	±3	°C	Internal
Voltage	0 to VCC	0.1	V	Internal
Tx Bias Current (Each Lane)	0 to 100	10%	mA	Internal
Tx Output Power (Each Lane)	-3.2 to +4.4	±3	dB	Internal
Rx Receive Power (Each Lane)	-7.2 to +4.4	±3	dB	Internal
Temperature	0 to 70	±3	°C	Internal

IX. Mechanical Diagram