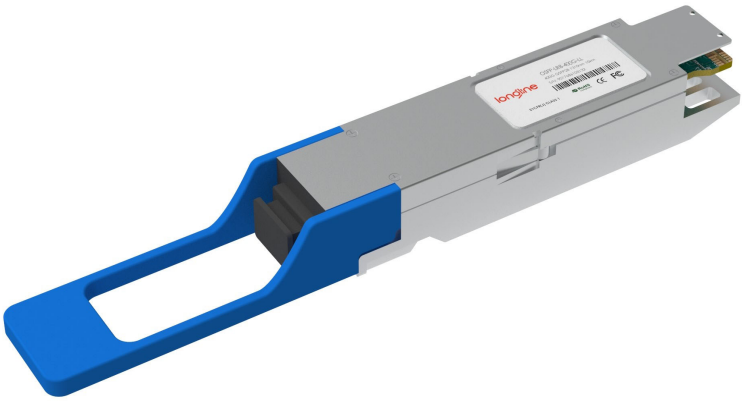
400GBase LR8 OSFP 1310nm 10km Duplex LC Transceiver

OSFP-LR8-400G-LL



Application

- 400G Ethernet
- Data Center and Enterprise Networking

Features

- Compliant with IEEE 802.3bs Standard:
  -400GBASE-LR8 Optical Interface
  -400GAUI-8 Electrical Interface
- Compliant with OSFP MSA HW Rev 2.0 with Duplex LC Connector
- Compliant with CMIS Rev 4.0
- Case Operating Temperature 0~70℃
- Two Wire Serial Interface with Digital Diagnostic Monitoring
- Complies with EU Directive 2011/65/EU
- Class 1 Laser

Product Description

The 400GBASE-LR8 module supports link lengths of up to 10km over single mode fiber (SMF) with duplex LC connector. It is compliant to ICMIS Rev 4.0, IEEE 802.3bs and OSFP MSA standard. The 400 Gigabit Ethernet signal is carried over eight wavelengths. Multiplexing and demultiplexing of the eight wavelengths are managed within the device.

Product Specifications

I. Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	T_S	-40	85	ºC
Supply Voltage	V_{CC}	-0.5	3.6	V
Relative Humidity (Non-condensing)	RH	5	95	%
Data Input Voltage Differential	$\|V_{DIP}-V_{DIN}\|$		1	V
Control Input Voltage	V_I	-0.3	V_{CC}+0.5	V
Control Output Current	I_O	-20	20	mA

II. Recommended Operating Environment

Parameter	Symbol	Min.	Typical	Max.	Unit
Operating Case Temperature	T_{OPR}	0		70	ºC
Power Supply Voltage	V_{CC}	3.135	3.3	3.465	V
Instantaneous Peak Current at Hot Plug	I_{CC_IP}			5600	mA
Sustained Peak Current at Hot Plug	I_{CC_SP}			4620	mA
Maximum Power Dissipation	PD			14	W
Maximum Power Dissipation, Low Power Mode	P_{DLP}			1.5	W

Parameter	Symbol	Min.	Typical	Max.	Unit
Signalling Speed per Lane	DRL		26.5625		GBd
Control Input Voltage High	V_{IH}	V_{CC}*0.7		V_{CC}+0.3	V
Control Input Voltage Low	V_{IL}	-0.3		V_{CC}*0.3	V
Two Wire Serial Interface Clock Rate				400	kHz
Power Supply Noise				66	mVpp
Rx Differential Data Output Load			100		Ohm
Operating Distance		2		10000	m

III. Electrical Characteristics

Parameter	Min.	Typical	Max.	Unit
Transmitter				
Differential Pk-pk Input Voltage Tolerance	900			mV
Differential Termination Mismatch			10	%
Single-ended Voltage Tolerance Range	-0.4		3.3	V
DC Common Mode Voltage	-350		2850	mV
Receiver				
AC Common-mode Output Voltage (RMS)			17.5	mV
Differential Output Voltage			900	mV
Near-end Eyeheight, Differential	70			mV

Parameter	Min.	Typical	Max.	Unit
Far-end Eye Height, Differential	30			mV
Far-end Pre-cursor Ratio			2.5	%
Differential Termination Mismatch			10	%
Transition Time (Min. 20%~80%)	9.5			ps
DC Common Mode Voltage	-350		2850	mV

IV. Optical Characteristics

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Transmitter						
Wavelength L0	λ_{C0}	1272.55	1273.55	1274.54	nm	
Wavelength L1	λ_{C1}	1276.89	1277.89	1278.89	nm	
Wavelength L2	λ_{C2}	1281.25	1282.26	1283.27	nm	
Wavelength L3	λ_{C3}	1285.65	1286.67	1287.68	nm	
Wavelength L4	λ_{C4}	1294.53	1295.56	1296.59	nm	
Wavelength L5	λ_{C5}	1299.02	1300.06	1301.09	nm	
Wavelength L6	λ_{C6}	1303.54	1304.59	1305.63	nm	
Wavelength L7	λ_{C7}	1308.09	1309.14	1310.19	nm	
Side Mode Suppression Ratio	SMSR	30			dB	
Total Average Launch Power	AOP_T			13.2	dBm	

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Average Launch Power, each lane	AOP_L	-2.8		5.3	dBm	1
Outer Optical Modulation Amplitude (OMA_{outer}), each Lane	T_{OMA}	0.2		5.7	dBm	
Difference in Launch Power Between Any Two Lanes (OMA_{outer})	D_{T_OMA}			4	dB	
Launch Power in OMA_{outer} Minus TDECQ, each Lane for ER>4.5dB	$T_{OMA-TDECQ}$	-1.2			dBm	
Launch Power in OMA_{outer} Minus TDECQ, each Lane for ER<4.5dB	TOMA-TDECQ	-1.1			dBm	
Transmitter and Dispersion Eye Closure for PAM4 (TDECQ), each Lane	TDECQ			3.3	dB	
Average Launch Power of OFF Transmitter, each Lane	T_{OFF}			-30	dBm	
Extinction Ratio	ER	3.5			dB	
$RIN_{15.1}$ OMA	RIN			-132	dB/Hz	
Optical Return Loss Tolerance	ORL			15.1	dB	
Transmitter Reflectance	T_R			-26	dB	2
	Receiver					
Wavelength L0	λ_{C0}	1272.55	1273.55	1274.54	nm	
Wavelength L1	λ_{C1}	1276.89	1277.89	1278.89	nm	
Wavelength L2	λ_{C2}	1281.25	1282.26	1283.27	nm	
Wavelength L3	λ_{C3}	1285.65	1286.67	1287.68	nm	
Wavelength L4	λ_{C4}	1294.53	1295.56	1296.59	nm	
Wavelength L5	λ_{C5}	1299.02	1300.06	1301.09	nm	

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Wavelength L6	λ_{C6}	1303.54	1304.59	1305.63	nm	
Wavelength L7	λ_{C7}	1308.09	1309.14	1310.19	nm	
Damage Threshold, each Lane	AOP_D	6.3			dBm	
Average Receive Power, each Lane	AOP_R	-9.1		5.3	dBm	
Receive Power (OMA_{outer}), each Lane	OMA_R			5.7	dBm	
Difference in Receive Power Between Any Two Lanes (OMA_{outer})	D_{R_OMA}			4.5	dB	
Receiver Reflectance	RR			-26	dB	
Receiver Sensitivity(OMA_{outer}), each Lane	S_{OMA}			-7.1	dBm	3
Stressed Receiver Sensitivity (OMA_{outer}), each Lane	SRS			-4.7	dBm	4

Notes

1. Average launch power, each lane (min) is informative and not the principal indicator of signal strength.
2. Transmitter reflectance is defined looking into the transmitte.
3. Receiver sensitivity (OMAouter), each lane (max) is informative and is defined for a transmitter with SECQ of 0.9 dB.
4. Measured with conformance test signal at TP3 for the BER = $2.4x10^{-4}$

V. Pin Description

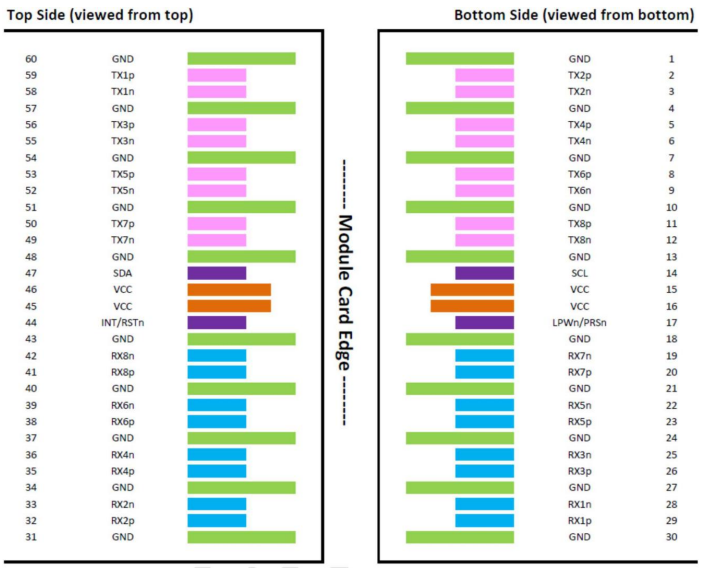


Figure 1 – Pin definitions of the module high speed inputs/outputs

Pin#	Symbol	Description	Logic	Pin#	Symbol	Description	Logic
1	GND	Ground		31	GND	Ground	
2	TX2p	Transmitter Data Non-Inverted	CML-I	32	RX2p	Receiver Data Non-Inverted	CML-O
3	TX2n	Transmitter Datal nverted	CML-I	33	RX2n	Receiver Data Inverted	CML-O
4	GND	Ground		34	GND	Ground	
5	TX4p	Transmitter Data Non-Inverted	CML-I	35	RX4p	Receiver Data Non-Inverted	CML-O
6	TX4n	Transmitter Data Inverted	CML-I	36	RX4n	Receiver Data Inverted	CML-O
7	GND	Ground		37	GND	Ground	
8	TX6p	Transmitter Data Non-Inverted	CML-I	38	RX6p	Receiver Data Non-Inverted	CML-O
9	TX6n	Transmitter Data Inverted	CML-I	39	RX6n	Receiver Data Inverted	CML-O
10	GND	Ground		40	GND	Ground	
11	TX8p	Transmitter Data Non-Inverted	CML-I	41	RX8p	Receiver Data Non-Inverted	CML-O
12	TX8n	Transmitter Datal nverted	CML-I	42	RX8n	Receiver Data Inverted	CML-O
13	GND	Ground		43	GND	Ground	
14	SCL	2-wire Serial Interface Cock	LVCMOS-I/O	44	INT/RSTn	Module Interrupt/Module Reset	Multi-Level
15	V_{CC}	3.3V Power		45	V_{CC}	3.3V Power	
16	V_{CC}	3.3V Power		46	V_{CC}	3.3V Power	
17	LPWn/PRSn	Low-Power Mode/Module Present	Multi-Level	47	SDA	2-wire Serial Interface Data	LVCMOS-I/O
18	GND	Ground		48	GND	Ground	
19	RX7n	Receiver Data Inverted	CML-O	49	TX7n	Transmitter Data Inverted	CML-I

Pin#	Symbol	Description	Logic	Pin#	Symbol	Description	Logic
20	RX7p	Receiver Data Non-Inverted	CML-O	**50**	TX7p	Transmitter Data Non-Inverted	CML-I
21	GND	Ground		**51**	GND	Ground	
22	RX5n	Receiver Data Inverted	CML-O	**52**	TX5n	Transmitter Data Inverted	CML-I
23	RX5p	Receiver Data Non-Inverted	CML-O	**53**	TX5p	Transmitter Data Non-Inverted	CML-I
24	GND	Ground		**54**	GND	Ground	
25	RX3n	Receiver Data Inverted	CML-O	**55**	TX3n	Transmitter Data Inverted	CML-I
26	RX3p	Receiver Data Non-Inverted	CML-O	**56**	TX3p	Transmitter Data Non-Inverted	CML-I
27	GND	Ground		**57**	GND	Ground	
28	RX1n	Receiver Data Inverted	CML-O	**58**	TX1n	Transmitter Datal nverted	CML-I
29	RX1p	Receiver Data Non-Inverted	CML-O	**59**	TX1p	Transmitter Data Non-Inverted	CML-I
30	GND	Ground		**60**	GND	Ground	

VI. Timing for Soft Control and Status Functions

Parameter	Symbol	Min.	Max.	Unit	Notes
MgmtInit Duration			2000	ms	
ResetL Assert Time	t_reset_init	10		µs	
IntL Assert Time	ton_IntL		200	ms	
IntL Deassert Time	toff_IntL		500	µs	
Rx LOS Assert Time (Fast Mode)	ton_losf		N/A	ms	Not Supported
Rx LOS Deassert (Fast Mode)	toff_losf		N/A	ms	Not Supported
Tx Fault Assert Time	ton_Txfault		200	ms	
Flag Assert Time	ton_flag		200	ms	
Mask Assert Time	ton_mask		100	ms	
Mask Deassert Time	toff_mask		100	ms	
Module Select Wait Time	ModSelL WaitTime		N/A		Not Supported

VII. I/O Timing for Squelch and Disable

Parameter	Symbol	Max.	Unit	Notes
Rx Squelch Assert Time	ton_Rxsq	15	ms	
Rx Squelch Deassert Time	toff_Rxsq	1500	ms	
Tx Squelch Assert Time	ton_Txsq	400	ms	
Tx Squelch Deassert Time	toff_Txsq	1000	ms	Based on Mdulation

Parameter	Symbol	Max.	Unit	Notes
Tx Disable Assert Time (Fast Mode)	ton_Txdisf	N/A	ms	Not Supported
Tx Disable Deassert Time(Fast Mode)	toff_Txdisf	N/A	ms	Not Supported
Rx Output Disable Assert Time	ton_Rxdis	100	ms	
Rx Output Disable Deassert Time	toff_Rxdis	100	ms	
Squelch Disable Assert Time	ton_sqdis	N/A	ms	Not Supported
Squelch Disable Deassert Time	toff_sqdis	N/A	ms	Not Supported

VIII. Digital Diagnostics

Parameter	Range	Accuracy	Unit	Calibration
Temperature	0~70	±3	ºC	Internal
Voltage	0~V_{CC}	0.1	V	Internal
Tx Bias Current (each Lane)	0~100	10%	mA	Internal
Tx Output Power (each Lane)	-2.8~5.3	±3	dB	Internal
Rx Receive Power (each Lane)	-9.1~5.3	±3	dB	Internal

IX. Diagram Mechanical Drawing

Unit: mm