10/25GBASE-SR SFP28 850nm 100m DOM Optical Transceiver Module

MMA2P00-AS-D-LL

Application

- 25G Ethernet
- 10G Ethernet

Features

- Compliant to SFP+ MSA
- Fully RoHS Compliant
- All metal housing for superior EMI performance
- Operating data rate up to 25.78Gbps
- Low power consumption <1.2 W
- High sensitivity Pin photodiode and TIA
- Up to 70m transmission on MMF OM3 and 100m transmission on MMF OM4
- LC duplex connector
- Hot pluggable 20pin connector
- Single +3.3V ± 5% power supply
- 0℃ to 70℃ operating wide temperature range
- Digital Monitoring SFF-8472 Rev 12.2 compliant
- 25G to 10G rate selection by turning off CDR

Description

The 10/25GBASE-SR module supports a link length of up to 70/100m over OM3/4 at both 10G and 25G.
They are compliant with SFF-8431,SFF-8432. The transmitter converts serial CML electrical data into serial optical data compliant with the IEEE802.3by standard. The receiver converts serial optical data into serial CML electrical data.Digital diagnostics functions are available via a 2-wire serial interface, as specified in SFF-8472.

Product Specifications

I. Absolute Maximum Ratings

Parameter	Symbol	Min	Typ.	Max	Unit	Ref.
Storage Temperature Range	Ts	0		70	℃	
Relative Humidity	RH	0		95	%	
Maximum Supply Voltage	Vcc3	-0.5		4.0	V	

II. General Specifications

Parameter	Symbol	Min	Typ.	Max	Unit	Ref.
Bit Rate	BR		25.78		Gb/s	1
Bit Error Ratio	BER					
Max. Supported Link Length	LMAX		100		m	

Note:

1.At 25.78Gb/s Ethernet data rate.

III. Recommended Operating Conditions

Parameter	Symbol	Min	Typ.	Max	Unit	Ref.
Operating Case Temperature Range	Tc	0		70	℃	
Power Supply Voltage	Vcc	3.14	3.3	3.46	V	

Bit Rate	BR		25.78		Gb/s	
Max. Supported Link Length	LMAX		100		m	

IV. Recommended Operating Environment

Parameter	Symbol	Min	Typ.	Max	Unit	Ref.
Supply Voltage	VCC	3.14	3.3	3.46	V	
Module Power	Icc			1200	mW	
Transmitter						
Input Differential Impedance	R_{IN}	80		120	Ω	
Differential Data Input	V_{IN}	150		1200	mVp-p	
Transmit Disable Voltage	V_{DIS}	2		V_{CCHOST}	V	
Transmit Enable Voltage	V_{EN}	V_{EE}		V_{EE}+0.8	V	
Transmit Fault Assert Voltage	V_{FA}	2		V_{CCHOST}	V	
Transmit Fault De-Assert Voltage	V_{FDA}	V_{EE}		V_{EE}+0.4	V	
Receiver						
Differential Data Output	V_{OD}	350		700	mVp-p	
Output Rise Time	t_{RISE}	25			pS	
Output Fall Time	t_{FALL}	25			pS	
LOS Fault	V_{LOSFT}	2		V_{CCHOST}	V	
LOS Normal	V_{LOSNR}	V_{EE}		V_{EE}+0.4	V	

V. Optical Characteristics (Tc=0 oC to 70 oC and Vcc= 3.14 to 3.46)

Parameter	Symbol	Min	Typ.	Max	Unit	Ref.
Transmitter						
Nominal Wavelength	λ		850		nm	
Optical Output Power	Pav	-5		2.4	dBm	
Extinction Ratio	ER	2			dB	
Optical Modulation Amplitude	OMA	-6.4		3	dBm	
Relative Intensity Noise	RIN			-128	dB/Hz	
Receiver						
Center Wavelength	λC		850		nm	
Receiver Sensitivity@25.78Gb/s	RSENSE			-10.3	dBm	1
Average Receiver Power	Pavg	-10.3		3	dBm	
Optical Return Loss			12		dB	
LOS Assert	LOSA	-30			dBm	
LOS De-Assert LOS	LOSD			-13	dBm	
LOS Hysteresis			0.5		dB	

Note:

1.Measured at ER>2dBm, PRBS 2^{31}-1 and BER better than or equal to 5E-5.

VI. Pin Assignment

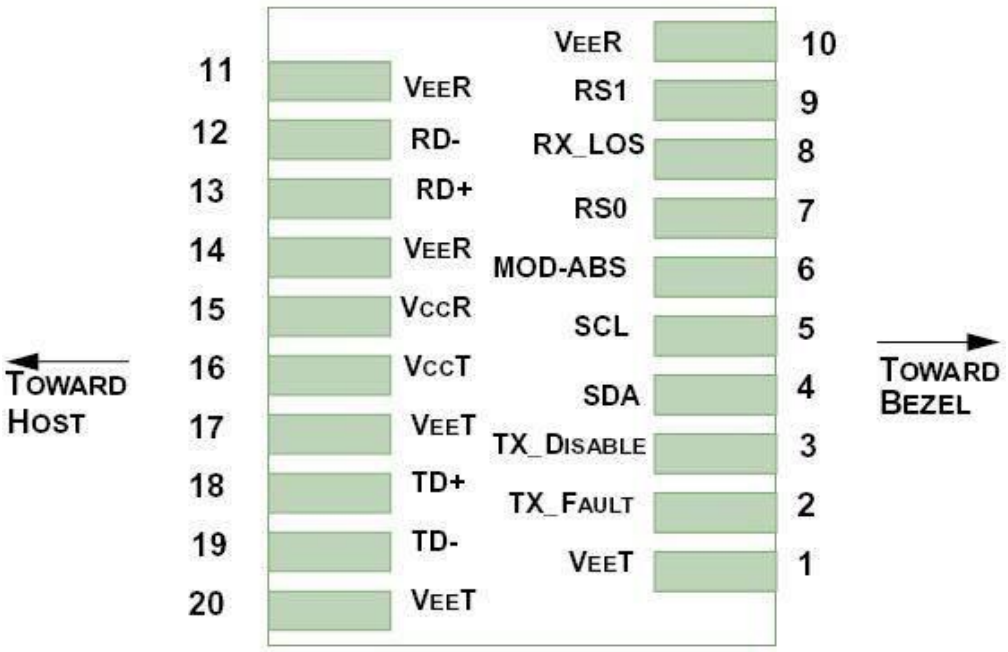
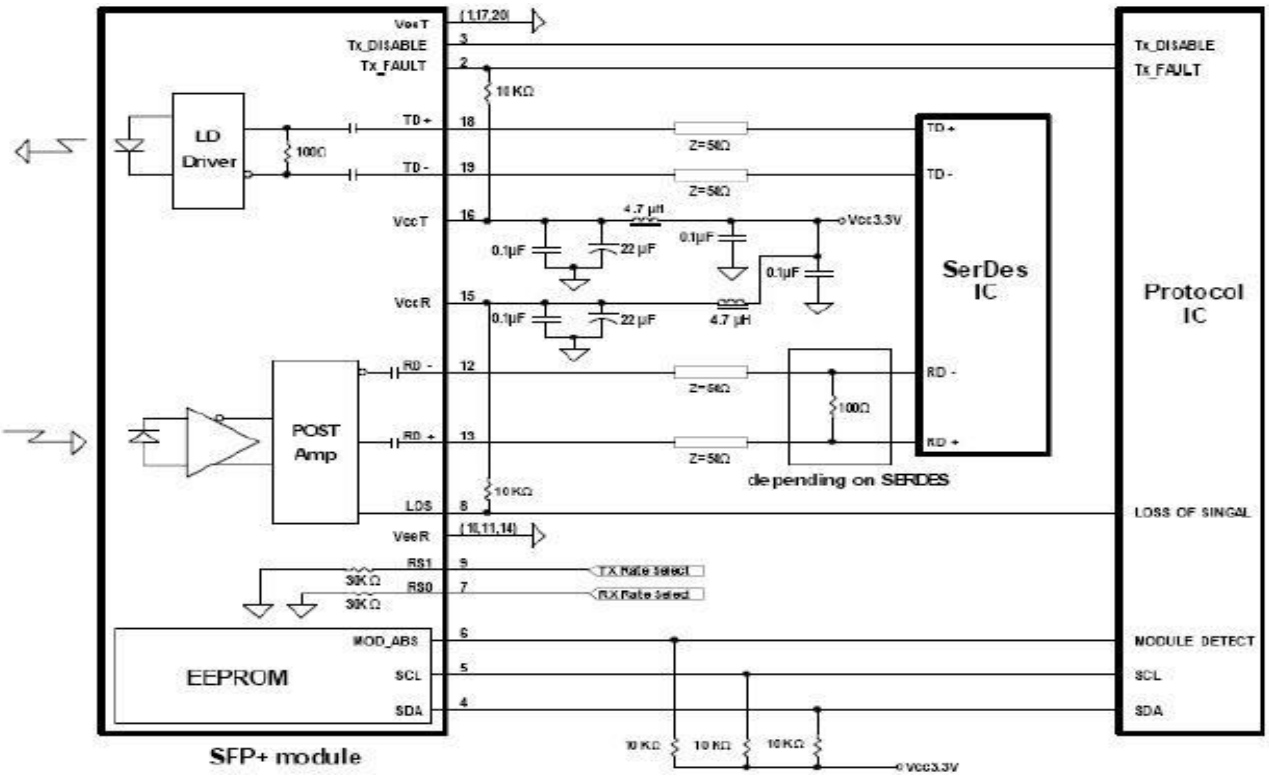


Figure 1 – Pin function definitions

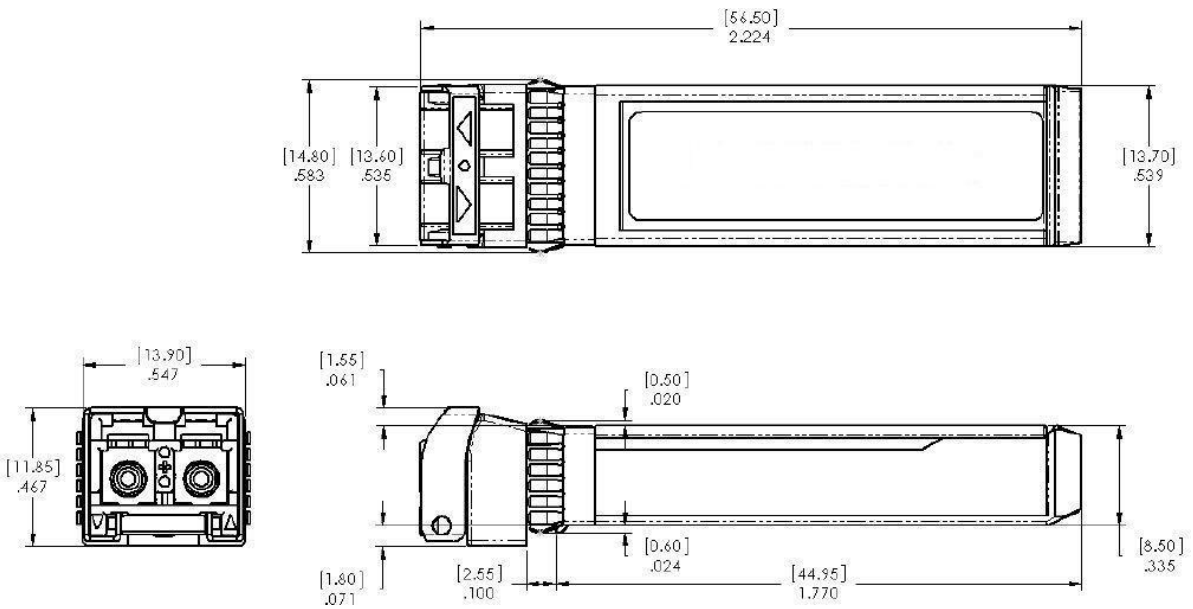
Pin	Symbol	Name	Description
1,17,20	VeeT	Transmitter Signal Ground	These pins should be connected to signal ground on the host board.
2	TX Fault	Transmitter Fault Out (OC)	Logic "1" Output = Laser Fault (Laser off before t_fault) Logic "0" Output = Normal Operation This pin is open collector compatible, and should be pulled up to Host Vcc with a 10kΩ resistor.
3	TX Disable	Transmitter Disable In (LVTTL)	Logic "1" Input (or no connection) = Laser off Logic "0" Input = Laser on This pin is internally pulled up to VccT with a 10 kΩ resistor.
4	SDA	Module Definition Identifiers	Serial ID with SFF 8472 Diagnostics Module Definition pins should be pulled up to Host Vcc with 10 kΩ resistors.
5	SCL		
6	MOD-ABS		
7	RS0	Receiver Rate Select (LVTTL) Transmitter Rate Select (LVTTL)	These pins have an internal 30kΩ pull-down to ground. A signal on either of these pins will not affect module performance.
9	RS1		
8	LOS	Loss of Signal Out (OC)	Sufficient optical signal for potential BER > 1x10-12 = Logic "0" Insufficient optical signal for potential BER < 1x10-12 = Logic "1" This pin is open collector compatible, and should be pulled up to Host Vcc with a 10kΩ resistor.

10,11,14	VeeR	Receiver Signal Ground	These pins should be connected to signal ground on the host board.
12	RD-	Receiver Negative DATA Out (CML)	Light on = Logic “0” Output Receiver DATA output is internally AC coupled and series terminated with a 50Ω resistor.
13	RD+	Receiver Positive DATA Out (CML)	Light on = Logic “1” Output Receiver DATA output is internally AC coupled and series terminated with a 50Ω resistor.
15	VccR	Receiver Power Supply	This pin should be connected to a filtered +3.3V power supply on the host board. See Figure 3.Recommended power supply filter
16	VccT	Transmitter Power Supply	This pin should be connected to a filtered +3.3V power supply on the host board. See Figure 3.Recommended power supply filter
18	TD+	Transmitter Positive DATA In (CML)	Logic “1” Input = Light on Transmitter DATA inputs are internally AC coupled and terminated with a differential 100Ω resistor.
19	TD-	Transmitter Negative DATA In (CML)	Logic “0” Input = Light on Transmitter DATA inputs are internally AC coupled and terminated with a differential 100Ω resistor.

VII. Optical Module Block Diagram



VIII. Diagram Mechanical Drawing



IX. Diagram Mechanical Drawing

As defined by the SFF-8472, Our SFP28 transceivers provide digital diagnostic functions via a 2-wire serial interface, which allows real-time access to the following operating parameters:

- Transceiver temperature
- Laser bias current
- Transmitted optical power
- Received optical power
- Transceiver supply voltage

It also provides a sophisticated system of alarm and warning flags, which may be used to alert
end-users when particular operating parameters are outside of a factory-set normal range. The operating and diagnostics information is monitored and reported by a Digital Diagnostics Transceiver Controller (DDTC) inside the transceiver, which is accessed through the 2-wire serial interface. When the serial protocol is activated, the serial clock signal (SCL pin) is generated by the host. The positive edge clocks data into the SFP28 transceiver into those segments of its memory map that are not write-protected. The negative edge clocks data from the SFP28 transceiver. The serial data signal (SDA pin) is bi-directional for serial data transfer. The host uses SDA in conjunction with SCL to mark the start and end of serial protocol activation. The memories are organized as a series of 8-bit data words that can be addressed individually or sequentially. The 2-wire serial interface provides sequential or random access to the 8 bit
parameters, addressed from 0x00h to the maximum address of the memory. For more detailed information, including memory map definitions , please see the SFF-8472 documentation1.