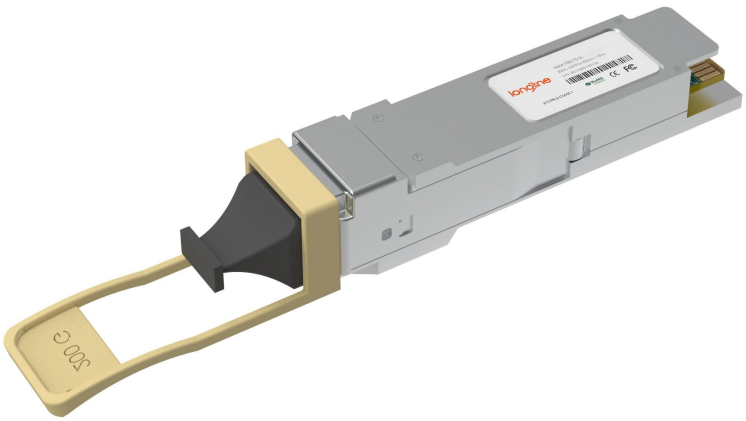
QSFP56 200GBASE-SR4 850nm 100m Transceiver

MMA1T00-VS-LL



Application

- 200GBASE-SR4 Ethernet
- Switch & Router Connections
- Data Centers
- Other 200G Interconnect Requirements

Features

- Up to 50Gbps data rate per channel by PAM4 modulation
- 4 duplex channels transmitters and receivers
- Integrated 850nm VCSEL array and PD array
- Single MPO-12 connector receptacle optical interface compliant
- Single +3.3V power supply
- DDM function implemented
- Hot-pluggable QSFP56 form factor
- Maximum link length of 100m on 12 core MPO OM4 (MMF) fiber
- Low power dissipation:<5W
- International class 1 laser safety certified
- Operating temperature range: 0℃ ~ +70 ℃
- Compliant with ROHS10

Description

The 200G QSFP56 SR4 Transceiver is designed to transmit and receive serial optical data links up to 50 Gb/s data rate (per channel) by PAM4 modulation format over multi-mode fiber. It is a small-form- factor hot pluggable transceiver module integrated with the high performance VCSEL laser and high sensitivity PIN receiver.

Product Specifications

I. Optical Characteristics

Parameter	Symbol	Unit	Min	Typ	Max	Notes
Transmitter (per Lane)						
Signaling Speed per Lane		GBd		26.5625 ± 100pm		
Modulation format				PAM4		
Center wavelength		nm	840	850	860	
RMS Spectral Width	SW	nm		0.6	0.6	
Average Launch Power per Lane	TXPx	dBm	-6.5		4	
Tx OMA per lane	TxOMA	dBm	-4.5		3	
aunch power in OMAouter minus TDECQ(min)		dBm	-5.9			
Optical Extinction Ratio	ER	dB	3			
Optical Return Loss Tolerance	ORL	dB			12	
Encircled Flux	FLX	dBm		>86% at 19um		
				<30%at 4.5um		
Transmitter and dispersion eye closure (TDECQ),each lane		dB			4.5	
Average launch power of OFF Transmitter, each lane		dBm			-30	
Receiver(per Lane)						
Signaling Speed per Lane		GBd		26.5625 ± 100pm		
Modulation format				PAM4		
Center wavelength		nm	840		860	
Damage Threshold	DT	dBm	5			
Average receive Power per Lane	RXPx	dBm	-8.4		4	
Receive power, each lane (OMAouter)		dBm			3	
Receiver reflectance	Rfl	dB			-12	
Stressed receiver sensitivity(OMAouter),each lane		dBm			-3.4	
Receiver sensitivity(OMAouter)each lane(SECQ=1.4dB)		dBm			-6.5	

II. Absolute Maximum Ratings

Parameter	Symbol	Unit	Min	Max
Storage Temperature Range	Ts	℃	-40	+85
Relative Humidity	RH	%	5	85
Power Supply Voltage	Vcc	V	-0.5	+4.0

III. Recommended Operating Conditions

Parameter	Symbol	Unit	Min	Typ	Max
Operating Case Temperature Range	Tc	oC	0	/	70
Power Supply Voltage	Vcc	V	3.135	3.3	3.465
Baud Rate(Per channel)	BR	GBd		26.5625	

IV. Optical Interface

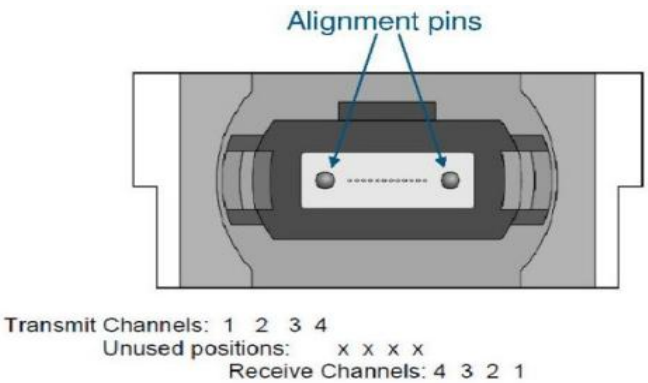


Figure 1. Optical lane sequence Note:

Optical interface is MPO-12.Lane sequence is shown in figure 1.

V. Principle diagram

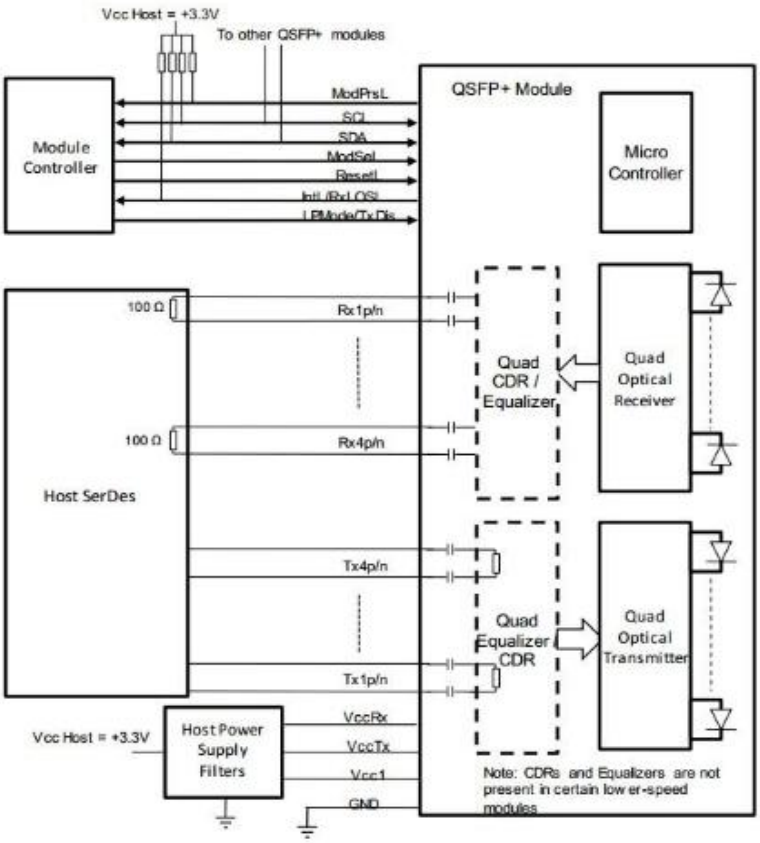


Figure 2. Module Principle Diagram

VI. Electric Ports Definition

Parameter	Symbol	Unit	Min	Typ	Max	Notes
Supply Voltage	VCC VCC3.3-Tx VCC3.3-Rx	V	3.135	3.3	3.465	
Power Consumption	Pc	W			5	
Transceiver Power-on Initialize Time		ms			2000	
Transmitter						
Differential peak-to-peak input voltage tolerance		mV	900			
Differential termination mismatch		%			10	
Differential input return loss(SDD11)		dB			See CEI-56G-VSR	

Common-mode to differential conversion and differential to common-mode conversion(SCD11,SDC11)		dB			See CEI-56G -VSR	
Receiver						
Differential peak-to-peak output voltage	·	mV			900	
DC Common Mode Voltage	Vcm	mV	-0.35		2.85	
AC Common Mode Noise, RMS		mV			17.5	
Differential termination mismatch		%			10	
Differential output return loss(SDD22)		dB			See CEI-56G -VSR	
Common-mode to differential conversion and differential to common-mode conversion(SCD22,SDC22)		dB			See CEI-56G -VSR	
IIC communication						
IIC Clock frequency	-	KHZ	/	400	1000	
clock stretching	-	us	/	/	500	
Data hold time	-	us	/	/	/	

VII. Pin Description

PIN	Logic	Symbol	DESCRIPTION	NOTE
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data output	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	

6	CML-I	Tx4p	Transmitter Non-Inverted Data output	
7		GND	Ground	1
8	LVTTL-I	ModSelL	Module Select	
9	LVTTL-I	ResetL	Module Reset	
10		VccRx	+3.3V Power Supply Receiver	2
11	LVCOMS-I/O	SCL	2-Wire Serial Interface Clock	
12	LVCOMS-I/O	SDA	2-Wire Serial Interface Data	
13		GND	Ground	1
14	CML-0	Rx3p	Receiver Non-Inverted Data Output	
15	CML-0	Rx3n	Receiver Inverted Data Output	
16		GND	Ground	1
17	CML-0	Rx1p	Receiver Non-Inverted Data Output	
18	CML-0	Rx1n	Receiver Inverted Data Output	
19		GND	Ground	1
20		GND	Ground	1
21	CML-0	Rx2n	Receiver Inverted Data Output	
22	CML-0	Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	1
24	CML-0	Rx4n	Receiver Inverted Data Output	
25	CML-0	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	1
27	CML-0	ModPrsL	Module Present	
28	CML-0	IntL/RxLOSL	Interrupt. Optionally configurable as RxLOSL via the management interface (SFF-8636)	
29		VccTx	+3.3 V Power Supply transmitter	2
30		Vcc1	+3.3 V Power Supply	2
31	LVTTL-I	LPMode/TxDis	Low Power Mode. Optionally configurable as TxDis via the management interface (SFF-8636).	
32		GND	Ground	1
33	CML-I	Tx3p	Transmitter Inverted Data Input	
34	CML-I	Tx3n	Transmitter Non-Inverted Data output	
35		GND	Ground	1
36	CML-I	Tx1p	Transmitter Inverted Data Input	
37	CML-I	Tx1n	Transmitter Non-Inverted Data output	
38		GND	Ground	1

Notes:

1. GND is the symbol for signal and supply (power) common for the QSFP28 module. All are common within the module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground plane.
2. VccRx, Vcc1 and VccTx are the receiving and transmission power suppliers and shall be applied concurrently. Recommended host board power supply filtering is shown in Figure 3 below. Vcc Rx, Vcc1 and Vcc Tx may be internally connected within the module in any combination. The connector pins are each rated for a maximum current of 1000mA.

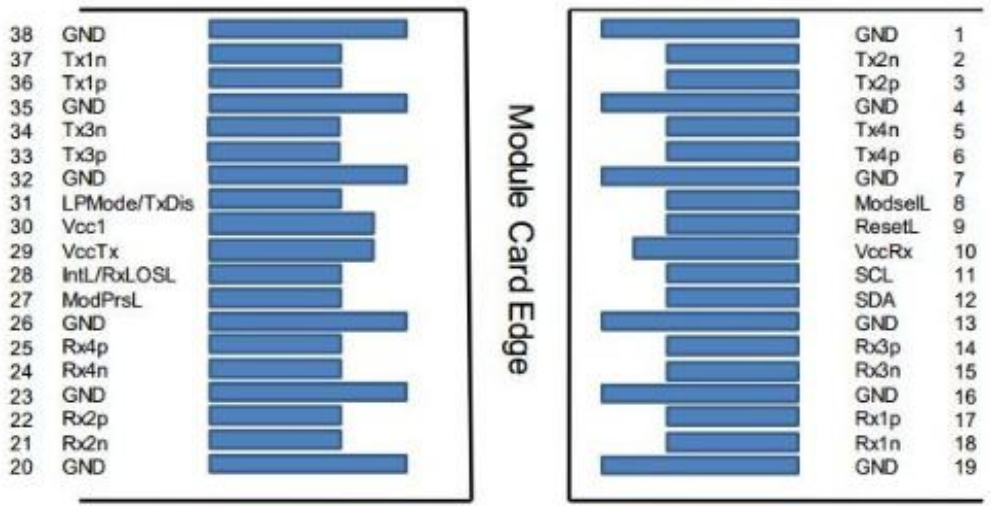
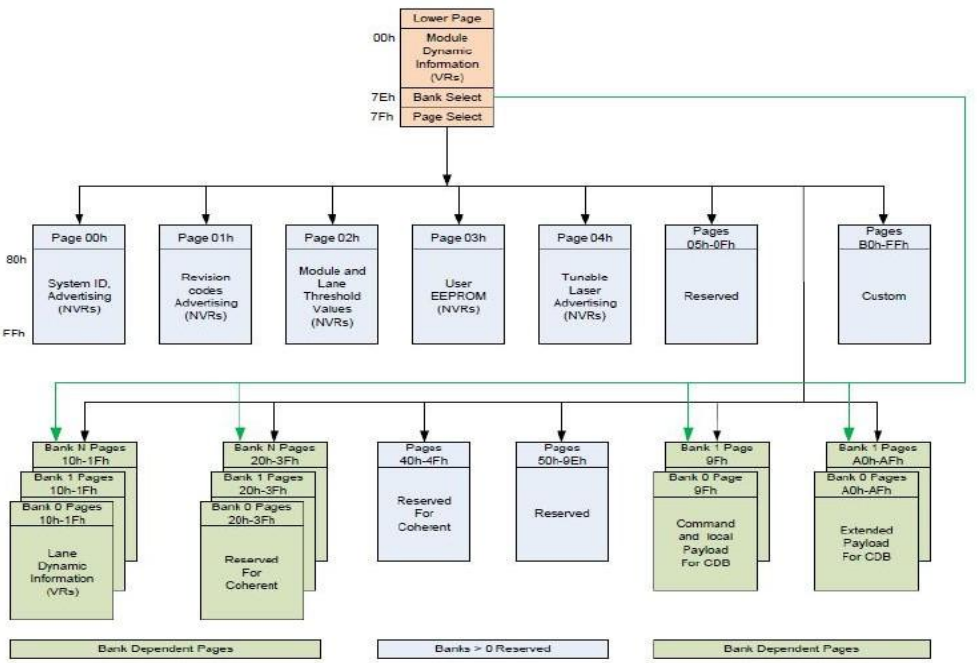


Figure 3. Electrical Pin-out Details

VIII. Module Memory Map



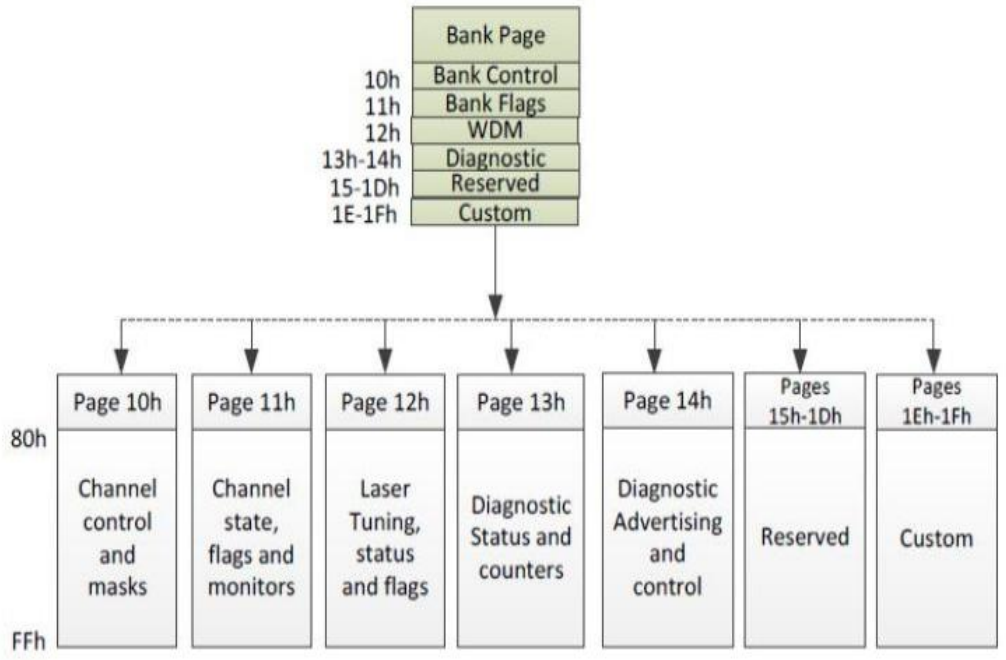


Figure 4 Digital Diagnostic Memory Map

IX. Host Board Power Supply Filtering

Any voltage drop across a filter network on the host is counted against the host DC set point accuracy specification. Inductors with DC resistance of less than 0.1 Ω should be used in order to maintain the required voltage at the host edge card connector. It is recommended that the 22 uF capacitors each have an equivalent series resistance of 0.22 Ω .The specification of the host power supply filtering network is beyond the scope of this specification, particularly because of the wide range of QSFP+ module Power Classes.Figure is the suggested transceiver/host interface.

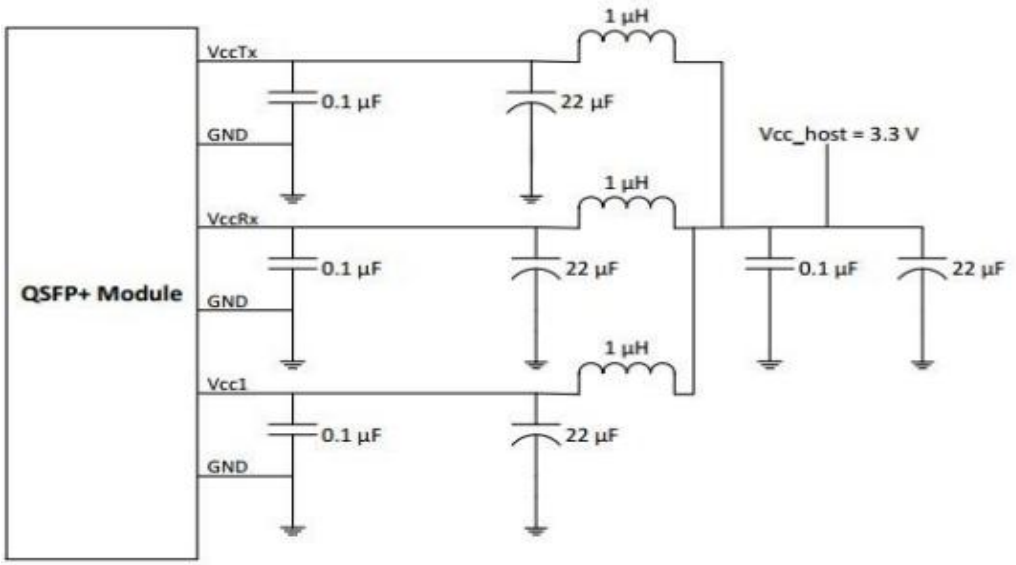


Figure 5 Recommended Host Board Power Supply Filtering

X. Package Outline

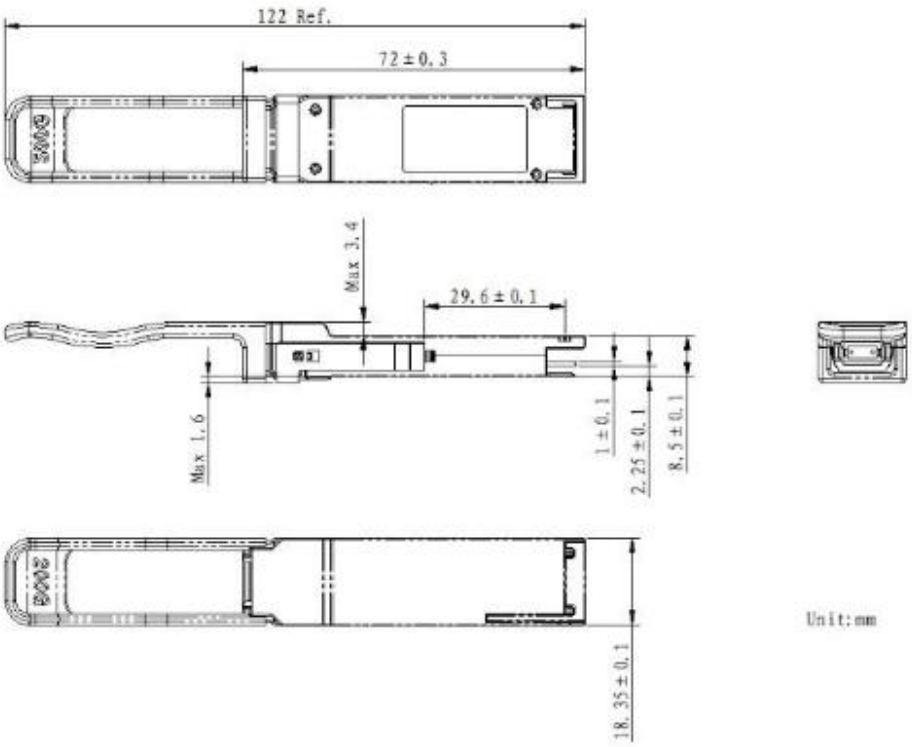


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Figure 6 Package Outline