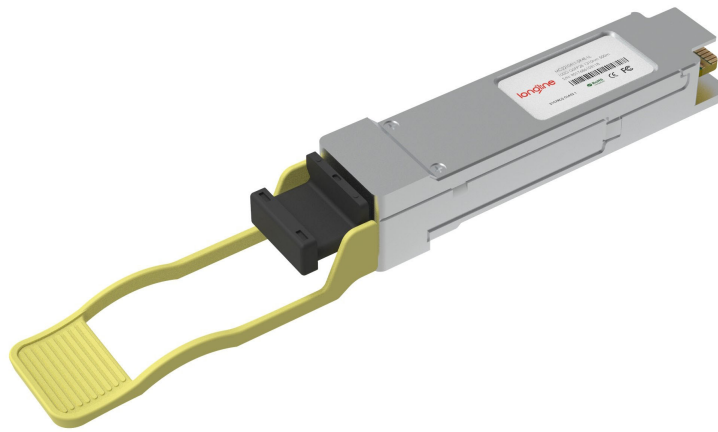**longline**

100G QSFP28 Passive Direct Attach Copper Twinax Cable for InfiniBand EDR

MC2210411-SR4E-LL

Application

- InfiniBand EDR

Standards

- IEEE 802.3bj 100GEBASE-CR4
- QSFP28 MSA
- SFF-8665
- SFF-8436

Features

- 4-Channel Full-Duplex Passive Copper Cable Transceiver
- Support Data Rates : 25.78Gb/s (per Channel)
- Maximum Aggregate Data Rate: 100Gb/s (4 x 25.78Gb/s)
- Copper Link x (x=0.5m, 1m, 1.5m, 2m, 3m)
- Low Power Consumption ≤0.5W

- 3.3V Single Power Supply
- Low Crosstalk
- I2C Based Two-wire Serial Interface for EEPROM Signature Which Can Be Customized
- Operating Temperature Range: 0~70℃

Description

The 100G QSFP28 to QSFP28 Passive Copper Cable assemblies are high performance, cost effective I/O solutions for LAN, HPC and SAN. The high speed cable assemblies meet and exceed 100 Gigabit Ethernet, InfiniBand EDR and temperature requirements for performance and reliability. The cables are compliant with SFF-8436 specifications and provide connectivity between devices using QSFP ports. It is suitable for short-distance connectivity within a rack or between adjacent racks in data centers.

Product Specification

I. Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating Case Temperature		-40		85	℃
Relative Humidity	T_C	0		70	℃
Supply Voltage	$V_{CC}3$	3.14	3.3	3.47	V
Data Rate per Lane		1		25.78	Gb/s

Note:

1. Damage may occur if the transceiver is subjected to conditions beyond the limits.
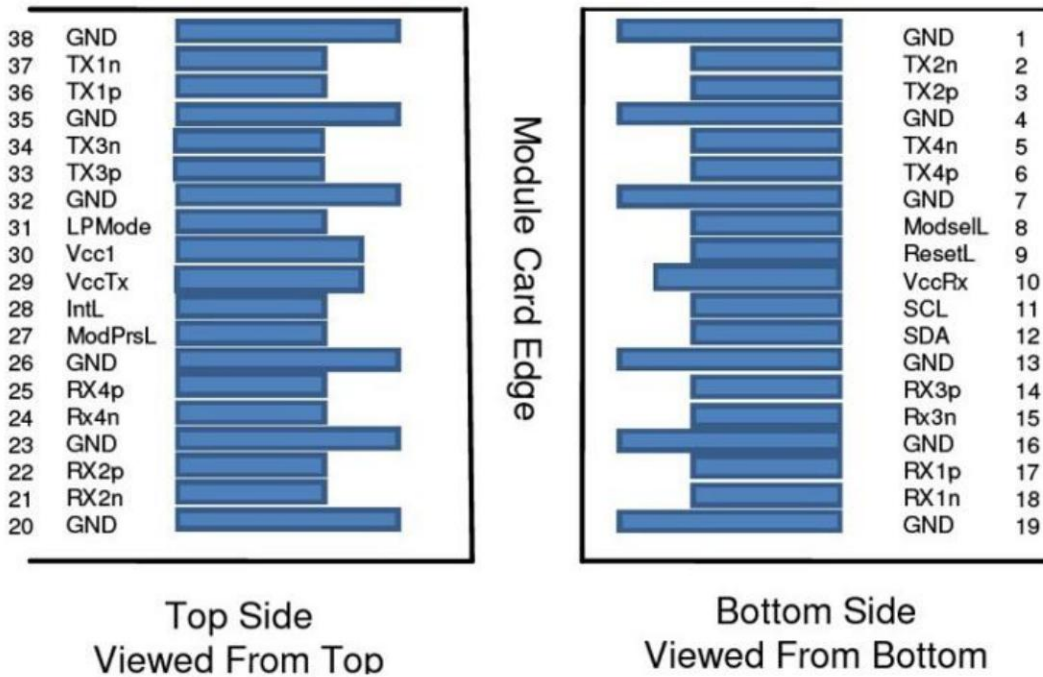
II. High Speed Characteristics

Parameter	Symbol	Min	Typ.	Max	Unit	Note
Differential Impedance	RIN, P	9	100	110	Ώ	
Insertion Loss	SDD2	8		22.48	dB	At 12.8906
Differential Return Loss	SDD11	12.45		See 1	dB	At 0.05 to
	SDD22	3.12		See 2		At 4.1 to 19
Common-mode to Common-mode Output Return Loss	SCC11 SCC22	2			dB	At 0.2 to 19 GHz
Differential to Common-mode Return Loss	SCD11	12		See 3	dB	At 0.01 to
	SCD22	10.58		See 4		At 12.89 to

Parameter	Symbol	Min	Typ.	Max	Unit	Note
Differential to Common-mode Conversion Loss	SCD21-IL	10				At 0.01 to
				See 5	dB	At 12.89 to
		6.3				At 15.7 to
Channel Operating Margin	COM	3			dB	

Notes:

1. Reflection Coefficient given by equation SDD11(dB) < 16.5 - 2 $\times$ SQRT(f), with finGHz.

2. Reflection Coefficient given by equation SDD11(dB) < 10.66 - 14 $\times$ log10(f/5.5), with finGHz.

3. Reflection Coefficient given by equation SCD11(dB) < 22 - (20/25.78)*f, with finGHz.

4. Reflection Coefficient given by equation SCD11(dB) < 15 - (6/25.78)*f, with finGHz.

5. Reflection Coefficient given by equation SCD21(dB) < 27 - (29/22)*f, with finGHz.

III. PIN Definitions

Top Side Viewed From Top		Bottom Side Viewed From Bottom	
38	GND	GND	1
37	TX1n	TX2n	2
36	TX1p	TX2p	3
35	GND	GND	4
34	TX3n	TX4n	5
33	TX3p	TX4p	6
32	GND	GND	7
31	LPMode	ModselL	8
30	Vcc1	ResetL	9
29	VccTx	VccRx	10
28	IntL	SCL	11
27	ModPrsL	SDA	12
26	GND	GND	13
25	RX4p	RX3p	14
24	Rx4n	Rx3n	15
23	GND	GND	16
22	RX2p	RX1p	17
21	RX2n	RX1n	18
20	GND	GND	19

Module Card Edge

**Top Side
Viewed From Top**

**Bottom Side
Viewed From Bottom**

Pin	Logic	Symbol	Description	Note
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data	
6	CML-I	Tx4p	Transmitter Non-Inverted	
7		GND	Ground	1
8	LVTTL-I	ModSelL	Module Select	
9	LVTTL-I	ResetL	Module Reset	
10		$V_{CC}Rx$	3.3V Power Supply	2
11	LVCMOS	SCL	2-Wire Serial Interface	
12	LVCMOS	SDA	2-Wire Serial Interface	
13		GND	Ground	1
14	CML-O	Rx3p	Receiver Non-Inverted	
15	CML-O	Rx3n	Receiver Inverted Data	
16		GND	Ground	1
17	CML-O	Rx1p	Receiver Non-Inverted	
18	CML-O	Rx1n	Receiver Inverted	
19		GND	Ground	1
20		GND	Ground	1

longline

Pin	Logic	Symbol	Description	Note
21	CML-O	Rx2n	Receiver Inverted Data	
22	CML-O	Rx2p	Receiver Non-Inverted	
23		GND	Ground	1
24	CML-O	Rx4n	Receiver Inverted Data	
25	CML-O	Rx4p	Receiver Non-Inverted	
26		GND	Ground	1
27	LVTTL-O	ModPrs	Module Present	
28	LVTTL-O	IntL	Interrupt	
29		VccTx	3.3V Power Supply	2
30		Vcc1	3.3V Power Supply	2
31	LVTTL-I	LPMode	Low Power Mode	
32		GND	Ground	1
33	CML-I	Tx3p	Transmitter Non-Inverted	
34	CML-I	Tx3n	Transmitter Inverted Data	
35		GND	Ground	1
36	CML-I	Tx1p	Transmitter Non-Inverted	1
37	CML-I	Tx1n	Transmitter Inverted Data	
38		GND	Ground	1

Notes:

1. GND is the symbol for signal and supply (power) common for the QSFP+ module. All are common within the QSFP+ module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the hostboard signal-common ground plane.

2. Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently. Requirements defined for the host side of the Host Edge Card Connector are listed in Table. Recommended host board power supply filter ing is shown in Figure. Vcc Rx Vcc1 and Vcc Tx may be internally connected within the QSFP+ Module module in any combination. The connector pins are each rated for a maximum current of 500 mA.
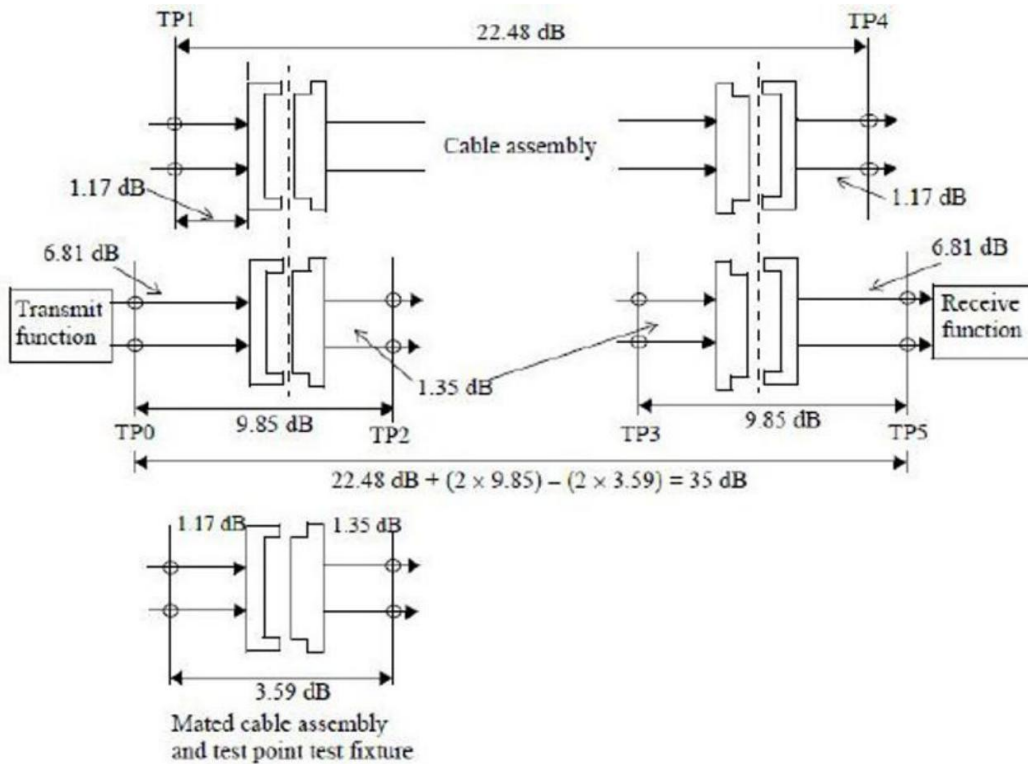
IV. Channel Insertion Loss Budget

Figure 2. 35dB Channel Insertion Loss Budget at 12.8906 GHz

Note:

1. The connector insertion loss is 1.07dB for the mated test fixture. The host connector is allocated 0.62dB of additional margin.

V. Mechanical Specifications

Unit: mm