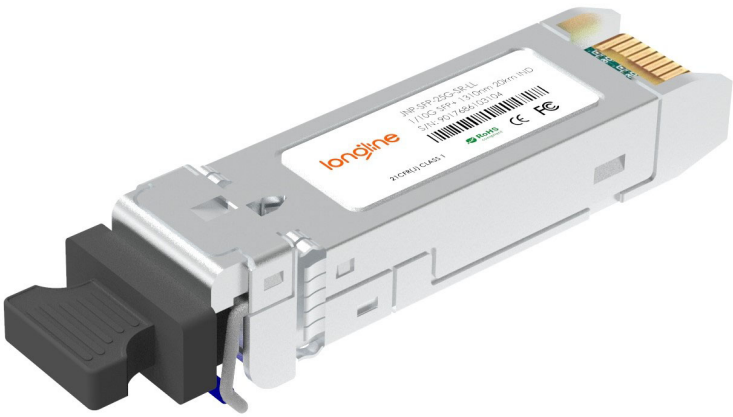
25G SFP28 850nm 300m DOM Transceiver

JNP-SFP-25G-SR-LL



Application

- Data Center Interconnect
- 25G BASE-ESR Ethernet

Features

- Supports 25.78Gb/s Bit Rate
- Hot-pluggable SFP28 Footprint
- 850nm VCSEL Laser and PIN Photo-detector
- Internal CDR on Transmitter and Receiver Channel
- Link Lengths at 25.78G 400m over OM4 MMF
- Link Lengths at 25.78G 300m over OM3 MMF
- LC Duplex Connector
- Low Power Consumption< 1W
- RoHS-10 Compliant (lead-free)
- 0℃ to 70℃ Operating Temperature Range
- Single +3.3V ± 5% Power Supply
- Programmable TX Input Equalizer
- Programmable RX

Description

The 25G ESR 300M short-wavelength transceiver is designed for using in 25.78Gb/s data rate over multimode fiber. The transceiver is compliant with SFF-8431, and the mechanical SFP28 plug is compatible with SFF-8432. Digital diagnostics functions are available via a 2-wire serial interface, as specified in SFF-8472.

Product Specifications

I. Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature Range	Ts	-40	85	℃
Relative Humidity	RH	0	85	%
Supply Voltage	V_{CC}	-0.3	4.0	V

II. Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating Case Temperature	T_{OPR}	0		70	℃
Power Supply Voltage	V_{CC}	3.14	3.3	3.46	V
Bit Rate	BR		25.78		Gb/s
Bit Error Ratio	BER			$5*10^{E-5}$	
Max Supported Link Length	L			300@OM3 400@OM4	m

III. Electrical Characteristics

Parameter	Symbol	Unit	Min.	Typ.	Max.	Note
Supply Voltage	V_{CC}	V	3.14	3.3	3.46	
Supply Current	Icc	mA			230	
Transmitter						
Input Differential Impedance	R_{IN}	Ω	80	100	120	1
Single Ended Data Input Swing	V_{IN}	mVp-p	90		500	
Transmit Disable Voltage	V_{DIS}	V	2		V_{CCHOST}	
Transmit Enable Voltage	V_{EN}	V	V_{EE}		V_{EE}+0.8	
Transmit Fault Assert Voltage	V_{FA}	V	2		V_{CCHOST}	
Transmit Fault De-Assert Voltage	V_{FDA}	V	V_{EE}		V_{EE}+0.8	
Receiver						
Single Ended Data Output Swing	V_{OD}	mVp-p	200		500	
LOS Fault	V_{LOSFT}	V	2		V_{CCHOST}	
LOS Normal	V_{LOSNR}	V	V_{EE}		V_{EE}+0.8	

Note:
1. Differential between TD+ / TD–

IV. Optical Characteristics

Parameter	Symbol	Unit	Min.	Typ.	Max.	Note
Transmitter						
Nominal Wavelength	λ	nm	840		860	
Spectral Width	Dl	nm			0.5	
Optical Modulation Amplitude	P_{OMA}	dBm	-4.3		3	
Optical Output Power	Pav	dBm	-6.4		2.4	
Extinction Ratio	ER	dB	2			
Transmitterand Dispersion Penalty	TDP	dB			5	
Average Launch Power of OFF Transmitter	P_{OFF}	dBm			-30	
Receiver						
Center Wavelength	λ	nm	840		860	
Average Receiver Power	PAVG	dBm	-10.3		2.4	1
Stressed Receiver Sensitivity (OMA)	R_{SENSE}	dBm			-5.2	2
Receiver Reflectance	R_{REFL}	dB			-12	
Assert LOS	LOS_A	dBm	-30			
De-Assert LOS	LOS_D	dBm			-13	
LOS Hysteresis		dB	0.5			

Notes:
1. Sensitivity for 25.78G PRBS 231-1 and BER better than or equal to $5*10^{E-5}$.
2. The stressed sensitivity value in the table is for system level BER measurements which include the effects of CDR circuit.

IV. Pin Function Definitions

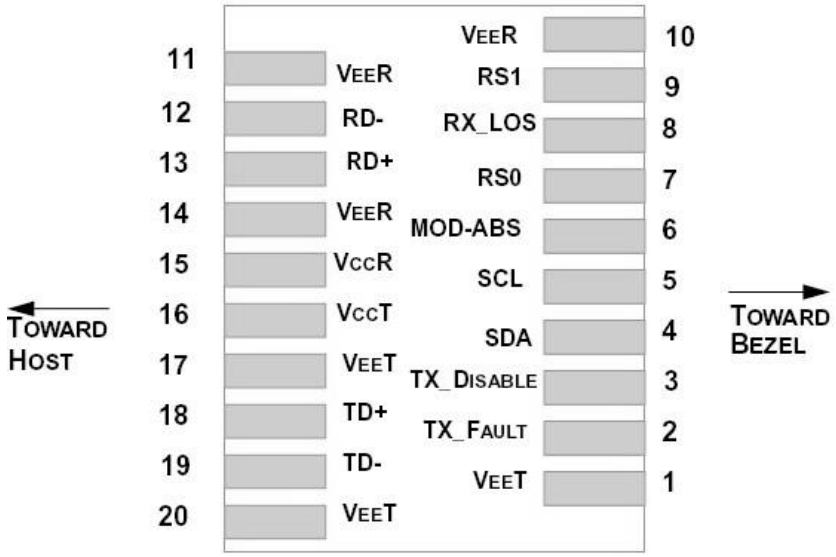


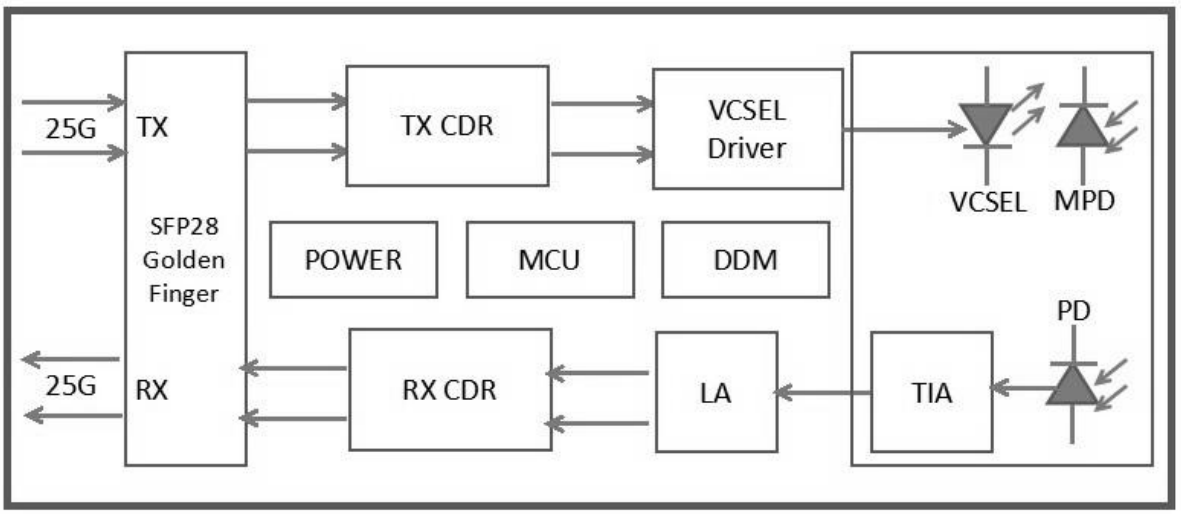
Figure1. Pin Definitions of the Module High Speed Inputs/Outputs

V. Transceiver Pin Descriptions

Pin No.	Symbol	Name	Definition
1,17,20	VeeT	Transmitter Signal Ground	Thesepins should be connected to signal ground on the host board.
2	TX Fault	Transmitter Fault Out (OC)	Logic "1" Output = Transmitter Fault Logic"0"Output= Normal Operation This pin is open collector compatible, and should be pulled up to Host Vcc with a 10kΩ resistor.
3	TX Disable	Transmitter Disable In (LVTTL)	Logic"1"Input(or no connection)=Laser off Logic"0"Input=Laser on This pin is internally pulled up to VccT with a 10kΩ resistor.
4	SDA	Module Definition Identifiers	SerialID with SFF8472 Diagnostics Module Definition pins should be pulled up to Host Vcc with 10kΩ resistors.
5	SCL		
6	MOD-ABS		

Pin No.	Symbol	Name	Definition
7	RS0	Receiver Rate Select (LVTTL) Transmitter Rate Select (LVTTL)	NA
9	RS1		
8	LOS	Loss of Signal Out (OC)	Thispin is open collector compatible, and should be pulled up to Host Vcc with a 10kΩ resistor.
10,11,14	VeeR	Receiver Signal Ground	These pins should be connected to signal ground on the host board.
12	RD-	Receiver Negative DATA Out (CML)	Light on = Logic "0" Output Receiver DATA output is internally AC coupled and series terminated with a 50Ω resistor.
13	RD+	Receiver Positive DATA Out (CML)	Light on = Logic "1" Output Receiver DATA output is internally AC coupled and series terminated with a 50Ω resistor.
15	VccR	Receiver Power Supply	This pin should be connected to a filtered +3.3V power supply on the host board. See Figure3. Recommended power supply filter
16	VccT	Transmitter Power Supply	This pin should be connected to a filtered +3.3V power supply on the host board. See Figure3. Recommended power supply filter
18	TD+	Transmitter Positive DATA In (CML)	Logic "1" Input = Light on Transmitter DATA inputs are internally AC coupled and terminated with a differential 100Ω resistor.
19	TD-	Transmitter Negative DATA In(CML)	Logic"0"Input = Light on Transmitter DATA inputs are internally AC coupled and terminated with a differential 100Ω resistor.

VI. Block Diagram



VII. Diagram Mechanial Drawing