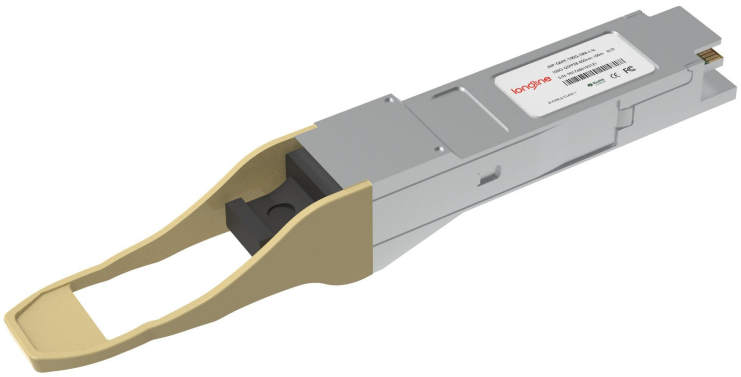
QSFP28 100GBASE-SR4 850nm 100m Industrial Transceiver

JNP-QSFP-100G-SR4-I-LL



Application

- 100GBASE-SR4 100G Ethernet
- Telecom Networking

Features

- Hot Pluggable QSFP28 form factor
- Supports 103.125Gb/s aggregate bit rate
- Maximum link length of 100m on OM4
- Multimode Fiber (MMF)
- Single MPO12 receptacle
- Single 3.3V power supply
- Typical Power Consumption ≤1.8W
- 4x25Gb/s 850mm VCSEL-based transmitter
- 4x25G electrical interface
- Industrial operating case temperature range: -40° C to 85° C
- I2C management interface
- RoHS-6 compliant

Description

100G QSFP28 transceiver modules are designed for use in100 Gigabit Ethernet links over multimode fiber. They are compliant with the QSFP28 MSA and IEEE 802.3bm 100GBASE-SR4 and CAUI-4. Digital diagnostics functions are available via the I2C interface, as specified by the QSFP28 MSA1and Finisar Application Note AN-2141. The transceiver is RoHS-6 compliant per Directive2011/65/EU.

Product Specifications

I. Absolute Maximum Ratings

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	V_{cc}	-0.3		3.6	V
Input Voltage	V_{in}	-0.3		Vcc+0.3	V
Storage Temperature	T_s	-20		85	ºC
Case Operating Temperature	T_c	-40		85	ºC
Humidity (non-condensing)	Rh	5		95	%

II. Recommended Operating Environment

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	V_{cc}	3.13	3.3	3.47	V
Operating Case Temperature	T_c	-40		85	ºC
Data Rate Per Lane	fd		25.78125		Gb/s
Humidity	Rh	5		85	%
Power Dissipation	P_m		1.8		W
Fiber Bend Radius	R_b	3			cm

III. Electrical Characteristics

Parameter	Symbol	Min	Typ.	Max	Unit
Differential Input Impedance	Z_{in}	90	100	110	ohm
Differential Output Impedance	Z_{out}	90	100	110	ohm
Differential Input Voltage Amplitude[1]	ΔV_{in}	300		1100	mVp-p
Differential Output Voltage Amplitude[2]	ΔV_{out}	500		800	mVp-p
Skew	Sw			300	ps
Bit Error Rate	BER		5×10-5		
Input Logic Level High	V_{IH}	2.0		Vcc	V
Input Logic Level Low	V_{IL}	0		0.8	V
Output Logic Level High	V_{OH}	Vcc-0.5		Vcc	V
Output Logic Level Low	V_{OL}	0		0.4	V

Notes:

1. Differential input voltage amplitude is measured between TxnP and TxnN.
2. Differential output voltage amplitude is measured between RxnP and RxnN.

IV. Optical Characteristics

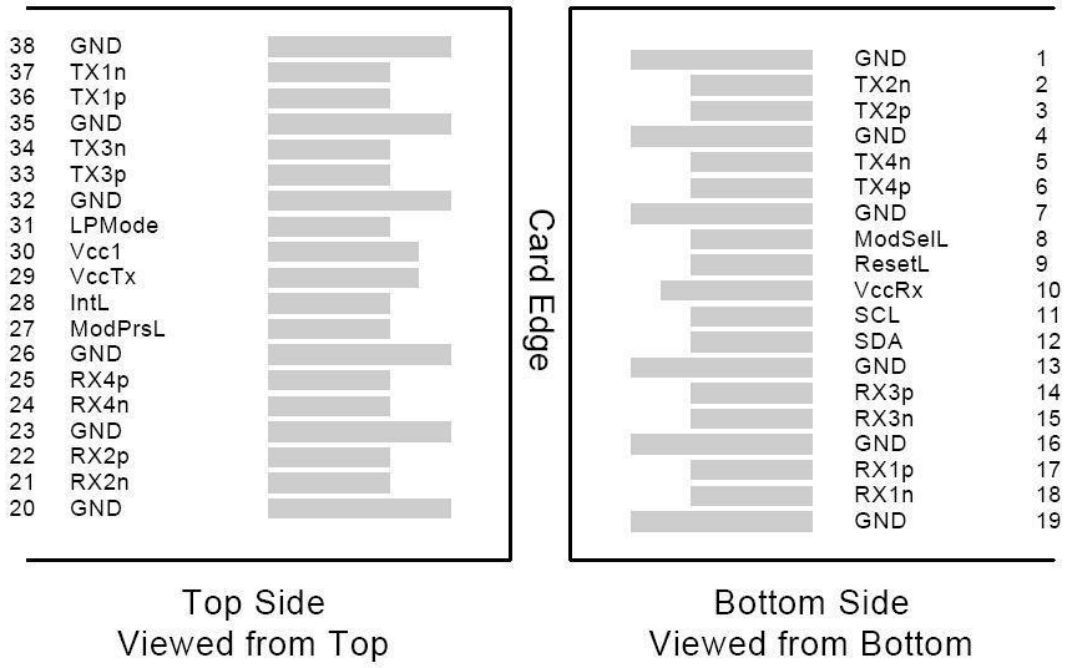
Parameter	Symbol	Min	Typ.	Max	Unit
Transmitter					
Center Wavelength	λ_c	840	850	860	nm
RMS Spectral Width	$\Delta\lambda$			0.6	nm
Average Launch Power (each lane)	P_{out}	-8.4		4.0	dBm
Optical Modulation Amplitude (each lane)	OMA	-6.4		3	dBm
Transmitter and Dispersion Eye Closure (each lane)	TDEC			4.3	dB
Extinction Ratio	ER	3			dB
Average Launch Power of OFF Transmitter (each lane)	P_{off}			-30	dB
Eye Mask Coordinates[1]: X1, X2, X3, Y1, Y2, Y3	{0.3, 0.38, 0.45, 0.35, 0.41, 0.5}				
Receiver					
Center Wavelength	λ_c	840	850	860	nm
Stressed Receiver Sensitivity in OMA_2				-5.2	dBm
Average Power at Receiver		-10.3		2.4	dBm
Receiver Reflectance	R_R			-12	dB
LOS Assert	LOS_A	-30			dBm
LOS De-Assert – OMA	LOS_D			-7.5	dBm
LOS Hysteresis	LOS_H	0.5			dB

Notes:

1. Hit Ratio = 5 × 10-5.

2. Measured with conformance test signal at TP3 for BER=5E-5.

V. Pin Assignment



Pin	Logic	Symbol	Description
1		GND	Module Ground[1]
2	CML-I	Tx2n	Transmitter inverted data input
3	CML-I	Tx2p	Transmitter non-inverted data input
4		GND	Module Ground[1]
5	CML-I	Tx4n	Transmitter inverted data input
6	CML-I	Tx4p	Transmitter non-inverted data input
7		GND	Module Ground[1]
8	LVTTL-I	ModSelL	Module Select[2]
9	LVTTL-I	ResetL	Module Reset[2]
10		VccRx	+3.3V Receiver Power Supply
11	LVCMOS-I	SCL	2-wire Serial interface data[2]
12	LVCMOS-I/O	SDA	2-wire serial interface data
13		GND	Module Ground[1]
14	CML-O	RX3p	Receiver non-inverted data output

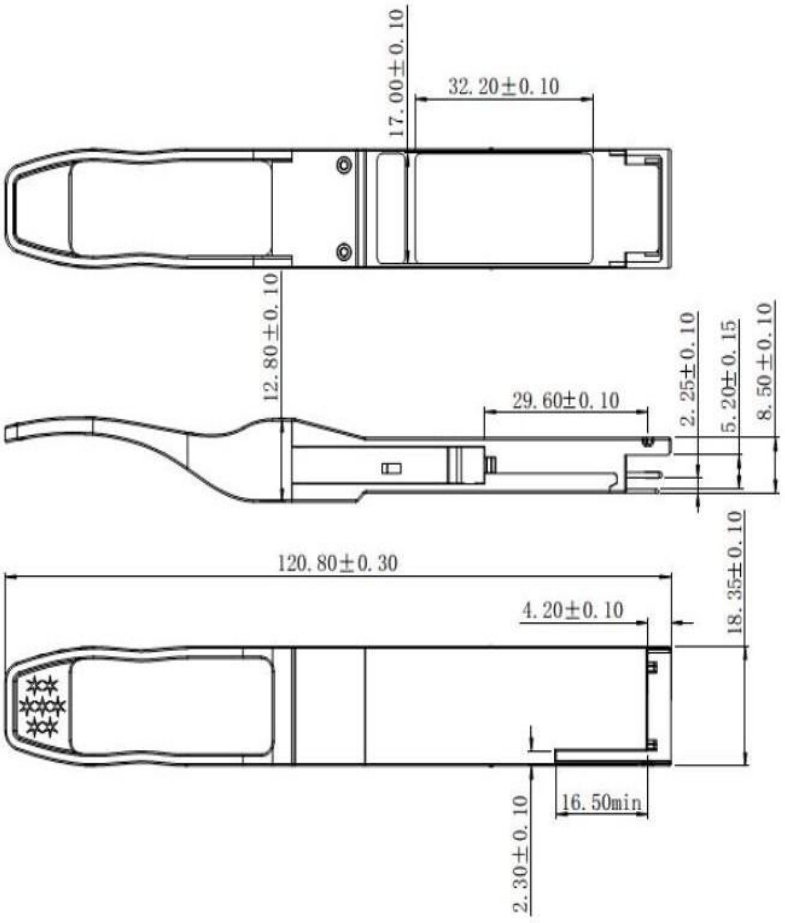
Pin	Logic	Symbol	Description
15	CML-O	RX3n	Receiver inverted data output
16		GND	Module Ground[1]
17	CML-O	RX1p	Receiver non-inverted data output
18	CML-O	RX1n	Receiver inverted data output
19		GND	Module Ground[1]
20		GND	Module Ground[1]
21	CML-O	RX2n	Receiver inverted data output
22	CML-O	RX2p	Receiver non-inverted data output
23		GND	Module Ground[1]
24	CML-O	RX4n	Receiver inverted data output
25	CML-O	RX4p	Receiver non-inverted data output
26		GND	Module Ground[1]
27	LVTTL-O	ModPrsL	Module Present, internal pulled down to GND
28	LVTTL-O	IntL	Interrupt output, should be pulled up on host board[2]
29		VCCTx	+3.3V Transmitter Power Supply
30		VCC1	+3.3V Power Supply
31	LVTTL-I	LPMode	Low Power Mode[2]
32		GND	Module Ground[1]
33	CML-I	Tx3p	Transmitter non-inverted data input
34	CML-I	Tx3n	Transmitter inverted data input
35		GND	Module Ground[1]
36	CML-I	Tx1p	Transmitter non-inverted data input
37	CML-I	Tx1n	Transmitter inverted data input
38		GND	Module Ground[1]

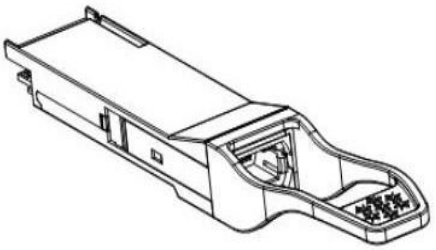
Notes:

1. Module circuit ground is isolated from module chassis ground within the module.

2. Open collector should be pulled up with 4.7K to 10K ohms on host board to a voltage between 3.15V and 3.6V.

VI. Diagram Mechanical Drawing





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