10GBASE-LR X2 1310nm 10km DOM Transceiver Module

J8437A-LL

Application

- 10GE Ethernet switches and routers
- 10GE Core-routers
- 10GE Storage
- Other 10Gbps Ethernet Transmission System

Features

- Compatible with X2 MSA Rev2.0b
- Support of IEEE 802.3ae 10GBASE-LR at 10.3125Gbps
- Transmission Distance up to 10Km(SMF)
- SC Receptacle 1310 DFB Laser
- Hot Pluggable 70-PIN Connector with XAUI Electrical Interface
- Management and control via MDIO 2-wire interface
- Power Supply :+3.3V, APS(+1.2V)
- Diagnostic Optics Monitoring
- Temperature Range: 0~ 70° C
- RoHS compliant

Description

The X2 LR is a highly integrated、Serial optical transponder module for high-speed, 10Gbit/s data transmission applications. 4×3.125Gbps Ethernet Signal Input by XAUI Interface.An integrated Coder / Decoder and multiplexer / demultiplexer (SERDES: Serializer / Deserializer). Designing for 300m Transmission with a vertical cavity surface emitting laser (VCSEL). Digital diagnostics functions are available via a 2-wire serial interface, as specified in the XENPAK MSA 3.0.

I. Absolute Maximum Ratings

Parameter	Symbol	Min	Typical	Unit	Ref.
Storage Ambient Temperature Range		-40	+85	° C	non condensing
Powered case Temperature Range		0	+70	° C	non condensing
Adaptable Power Supply (APS)	Vapsense	0	1.5	V	Voltage @ Pin APS Sense
Supply Voltage Range @ 3.3V	Vcc3	-0.5	4.0	V	

Any stress beyond the maximum ratings can result in permanent damage. The device specifications are guaranteed only under the recommended operating conditions.

II. Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Operating Case Temperature	Tc	0		+70	° C
Power Supply Voltage	V_{CC3}	3.14	3.0	3.47	V
	V_{APS}	1.152	1.2	1.248	
Power Dissipation	PD		3.5	4	W

III. XAUI I/O Characteristics

Parameter	Symbol	Min	Typ.	Max	Unit	Note
XAUI Date Rate	DR		3.125		Gb/s	
XAUI Baud Rate Tolerance		-100		+100	ppm	Relative Tolerance
Differential Input Voltage Swing		220		1600	mv	8B/10B Coded Input Signal
Differential Output Voltage Swing		800		1600	mVp-p	RLOAD = 100Ω ± 5%

Differential Input Impedance		80	100	120	Ω	
Total Output Jitter	TJXAUI			0.35	UI	no pre-equalization
Total Deterministic Output Jitter	DJXAUI			0.17	UI	no pre-equalization

IV. Optical Interface

Transmitter Characteristics

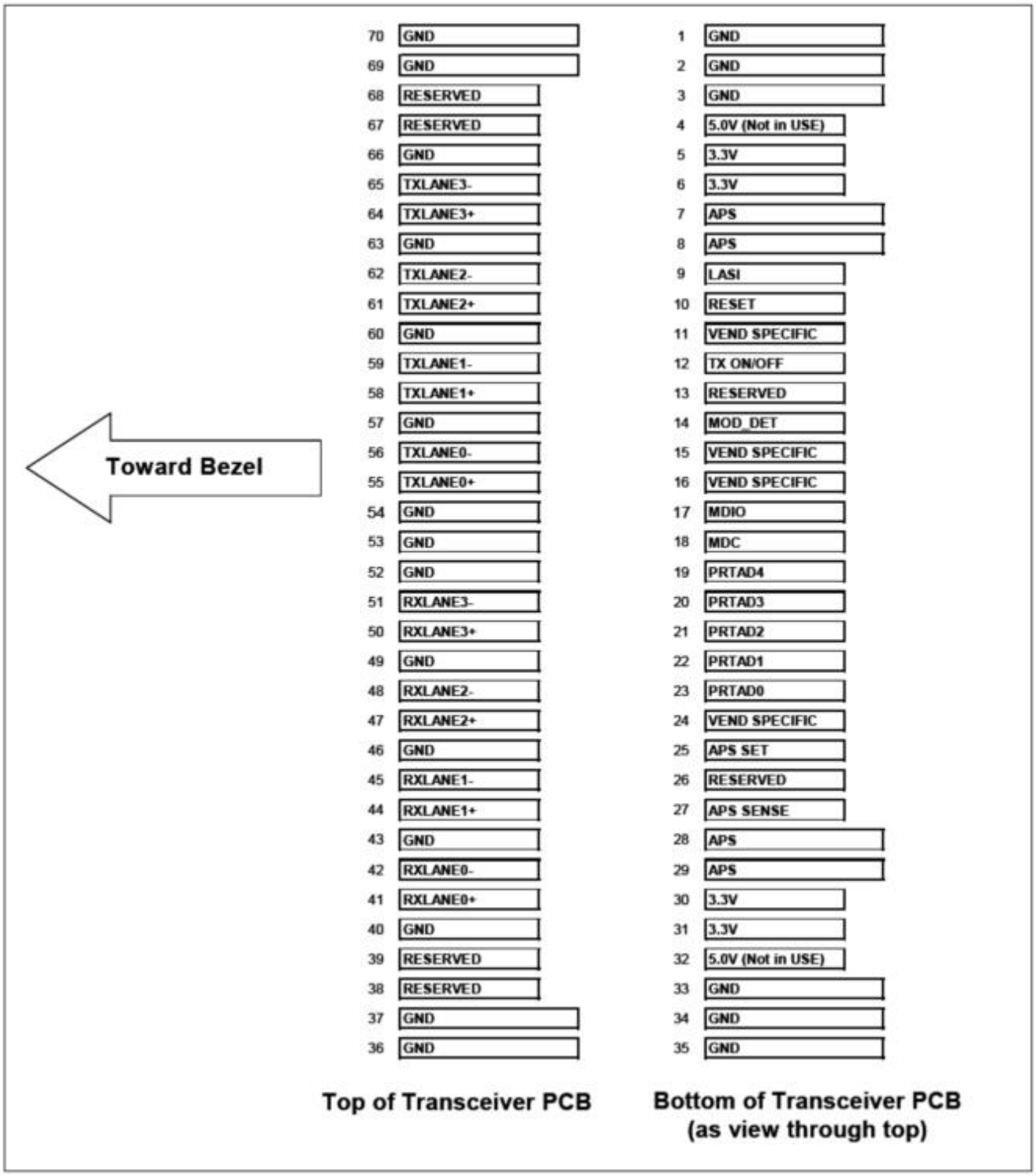
Parameter	Symbol	Min	Typ.	Max	Unit	Note
Operating Range				10	Km	
Operating Date Rate			10.3125		Gb/s	
Overload	Po	-8.2		0.5	dBm	
Input Centre Wavelength	λ	1260	1310	1255	nm	
SMSR.	SWSR	30			dB	
Extinction Ratio	ER	3.5	6			
Optical Modulation Amplitude	OMA	500			μW	
Transmitter and Dispersion Penalty	TDP			3.2	dB	

Receiver Characteristics

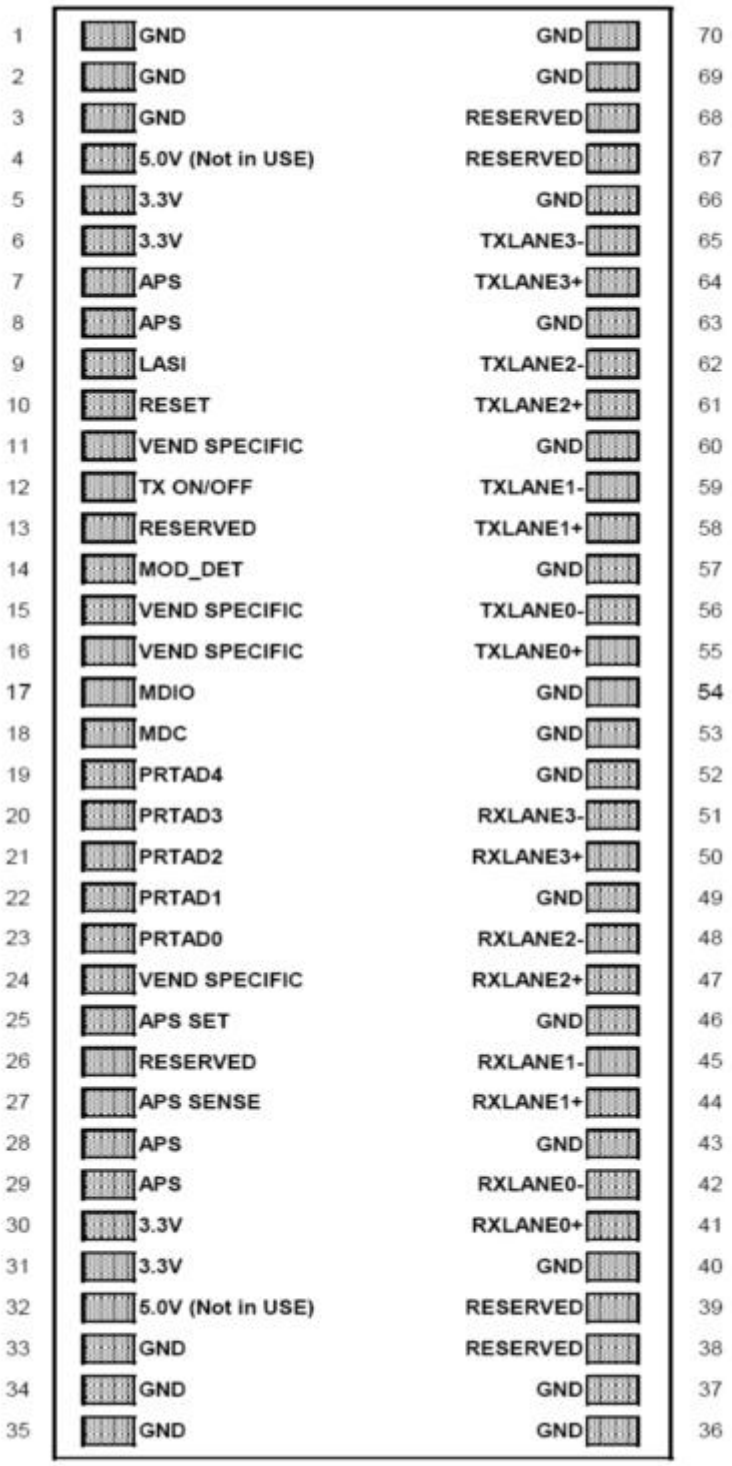
Parameter	Symbol	Min	Typ.	Max	Unit	Note
Operating Date Rate			10.3125		Gb/s	
Overload	Po	0.5			dBm	
Sensitivity in OMA	OMA0			-12.6	dBm	
Stressed Sensitivity in OMA	OMAst			-10.3	dBm	
Sensitivity MINI	Pmin			-14.4	dBm	1

Note :1. Measured at 10.3125Gb/s,Non-framed PRBS2^31-1,NRZ

V. Electrical PAD Layout



VI. Host PCB X2 PINOUT



1	GND	GND	70
2	GND	GND	69
3	GND	RESERVED	68
4	5.0V (Not in USE)	RESERVED	67
5	3.3V	GND	66
6	3.3V	TXLANE3-	65
7	APS	TXLANE3+	64
8	APS	GND	63
9	LASI	TXLANE2-	62
10	RESET	TXLANE2+	61
11	VEND SPECIFIC	GND	60
12	TX ON/OFF	TXLANE1-	59
13	RESERVED	TXLANE1+	58
14	MOD_DET	GND	57
15	VEND SPECIFIC	TXLANE0-	56
16	VEND SPECIFIC	TXLANE0+	55
17	MDIO	GND	54
18	MDC	GND	53
19	PRTAD4	GND	52
20	PRTAD3	RXLANE3-	51
21	PRTAD2	RXLANE3+	50
22	PRTAD1	GND	49
23	PRTAD0	RXLANE2-	48
24	VEND SPECIFIC	RXLANE2+	47
25	APS SET	GND	46
26	RESERVED	RXLANE1-	45
27	APS SENSE	RXLANE1+	44
28	APS	GND	43
29	APS	RXLANE0-	42
30	3.3V	RXLANE0+	41
31	3.3V	GND	40
32	5.0V (Not in USE)	RESERVED	39
33	GND	RESERVED	38
34	GND	GND	37
35	GND	GND	36

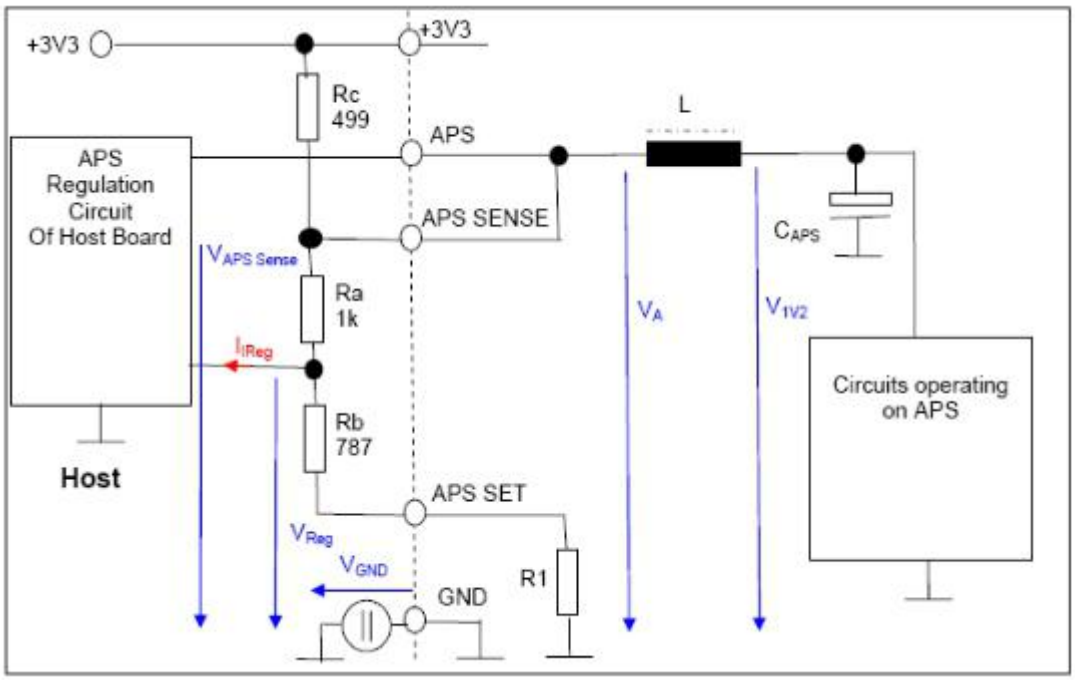
VII. Pin Function Definitions

PIN NO	Name	Dir	Logic	Function	Notes
1	GND			Electrical Ground	
2	GND			Electrical Ground	
3	GND			Electrical Ground	
4	5.0V			Power	
5	3.3V			Power	
6	3.3V			Power	
7	APS			Adaptive Power Supply	
8	APS			Adaptive Power Supply	
9	LASI	O	1.2V CMOS Open Drain	Link Alarm Status Interrupt, low active, Open Drain Output A pull-up resistor with 10-22KΩ to 1,2V is expected. Logic High: Normal Operation Logic Low: Link Alarm is indicated	
10	Reset	I	1.2V CMOS Open Drain	Low active Reset Input 10KΩ pull-up on Transceiver Logic high = Normal Operation Logic Low = Reset asserted	
11	VEND SPECIFIC			Vendor Specific Pin,. leave unconnected	
12	TX ON/OFF	I	1.2V CMOS Open Drain	High active Transmitter Enable Input 10KΩ pull-up on Transceiver Logic high = Transmitter active (normal Operation) And Register Bit 1.9.0 set to low as well Logic Low = shut down of Transmitter	
13	RESERVED			RESERVED	
14	MOD DETECT	O		1kΩ to Ground On Transceiver	
15	VEND SPECIFIC			Vendor Specific Pin,. leave unconnected	
16	VEND SPECIFIC			Vendor Specific Pin,. leave unconnected	
17	MDIO	I/O	1.2V CMOS	Management Data I/O. Requires external 10-22 kΩ pull-up to 1.2 V on host.	
18	MDC	I	1.2V CMOS	Management Clock Input	
19	PRTAD4	I		Port Address Bit 4(LOW=0)	
20	PRTAD3	I		Port Address Bit 3(LOW=0)	

21	PRTAD2	I		Port Address Bit 2(LOW=0)	
22	PRTAD1	I		Port Address Bit 1(LOW=0)	
23	PRTAD0	I		Port Address Bit 0(LOW=0)	
24	VEND SPECIFIC			Vendor Specific Pin,. leave unconnected	
25	APS SET	I		Feedback Input for APS, Input of APS Setting Resistor	
26	RESERVED			RESERVED	
27	APS SENSE	O		APS Sense Output for APS Control Circuit	
28	APS			Adaptive Power Supply	
29	APS			Adaptive Power Supply	
30	3.3V			Power	
31	3.3V			Power	
32	5.0V			Power	
33	GND			Electrical Ground	
34	GND			Electrical Ground	
35	GND			Electrical Ground	
36	GND			Electrical Ground	
37	GND			Electrical Ground	
38	RESERVED			RESERVED	
39	RESERVED			RESERVED	
40	GND			Electrical Ground	
41	RX LANE 0+			Module XAUI Output Lane 0+	
42	RX LANE 0-			Module XAUI Output Lane 0-	
43	GND			Electrical Ground	
44	RX LANE 1+			Module XAUI Output Lane 1+	
45	RX LANE 1-			Module XAUI Output Lane 1-	
46	GND			Electrical Ground	
47	RX LANE 2+			Module XAUI Output Lane 2+	
48	RX LANE 2-			Module XAUI Output Lane 2-	

49	GND			Electrical Ground	
50	RX LANE 3+			Module XAUI Output Lane 2+	
51	RX LANE 3-			Module XAUI Output Lane 2-	
52	GND			Electrical Ground	
53	GND			Electrical Ground	
54	GND			Electrical Ground	
55	RX LANE 0+			Module XAUI Output Lane 0+	
56	RX LANE 0-			Module XAUI Output Lane 0-	
57	GND			Electrical Ground	
58	TX LANE 1+			Module XAUI Output Lane 1+	
59	TX LANE 1-			Module XAUI Output Lane 1-	
60	GND			Electrical Ground	
61	TX LANE 2+			Module XAUI Output Lane 2+	
62	TX LANE 2-			Module XAUI Output Lane 2-	
63	GND			Electrical Ground	
64	TX LANE 3+			Module XAUI Output Lane 2+	
65	TX LANE 3-			Module XAUI Output Lane 2-	
66	GND			Electrical Ground	
67	RESERVED			RESERVED	
68	RESERVED			RESERVED	
69	GND			Electrical Ground	
70	GND			Electrical Ground	

VIII. Block Diagram of Adapter Power Supply Circuit



IX. Package Dimensions