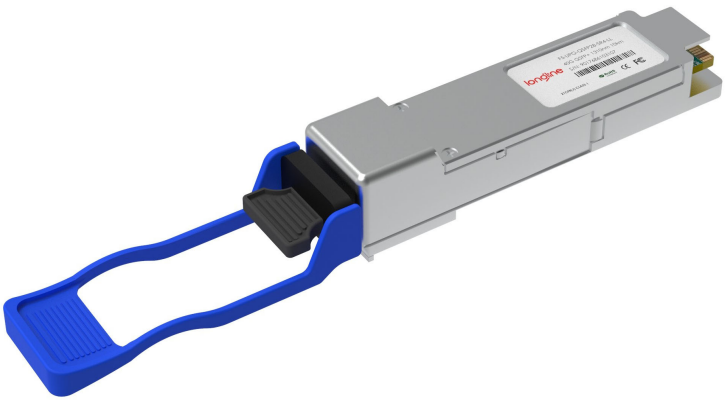
QSFP28 100GBASE-SR4 850nm 100m Transceiver

F5-UPG-QSFP28-SR4-LL



Application

- 100GBASE-SR4 100G Ethernet

Features

- Hot Pluggable QSFP28 form factor
- Supports 103.1Gb/s aggregate bit rate
- Maximum link length of 100m on OM4 Multimode Fiber (MMF)
- Single MPO12 receptacle
- Single 3.3V power supply
- Typical Power dissipation <1.8W
- 4x25Gb/s 850mm VCSEL-based transmitter
- 4x25G electrical interface
- Commercial operating case temperature range: 0° C to 70° C
- I2C management interface
- RoHS-6 compliant

Product Specifications

I. Absolute Maximum Ratings

Parameter	Symbol	Unit	Min	Max
Storage Temperature Range	Ts	ºC	-40	85
Relative Humidity (non-condensing)	RH	%	5	95
Supply Voltage	Vcc	V	-0.5	3.6

II. Recommended Operating Conditions

Parameter	Symbol	Min	Type	Max	Unit	Notes
Operating Case Temperature	TOPR	0		70	ºC	
Relative Humidity (non-condensing)	RH	5		85	%	
Power Supply Voltage	Vcc	3.135	3.3	3.465	V	
Total Power Consumption	Pc			2.5	W	
Supply current				750	mA	
Operating Distance				70	m	OM3
				100	m	OM4

III. Electrical Characteristics (Tc=-40℃ to 85℃ and Vcc= 3.135 to 3.465V)

Parameter	Unit	Symbol	Min	Type	Max
Supply Voltage	V	Vcc	3.135		3.465

Supply Current	A	Icc			1.5
Module total power	W	P		1.8	
Transmitter					
Signaling rate per lane	Gb/s	25.78125 ± 100ppm			
Differential pk-pk input voltage tolerance	mV	Vin pp diff			900
Single-ended voltage tolerance	v	Vin pp	-0.35		3.3
Module stress input test		Per Section 83E.3.4.1,IEEE 802.3 bm			
Receiver					
Signaling rate per lane	Gb/s	25.78125 ± 100ppm			
Differential data output swing	mVpp	Vout pp	100		400
			300		600
			400		800
			600		1200
Eye width	Ui		0.57		
Eye height, differential	mV		288		
Vertical eye closure	dB	VEC	5.5		
Transition time(20% to 80%)	ps	tr tf	12		

NOTE:

1.Maximum total power value is specified across the full operational temperature and voltage range when CDRs are locked or a lack of input signal results in squelch being activated If incorrect frequencies cause the CDRs to continuously attempt to lock maximum power dissipation may reach 4.5W

2.Output voltage is settable in 4 discrete ranges via I2C Default range is Range2.Output voltag

IV. Transmitter Optical Specifications

Parameter	Symbol	Min	Type	Max	Unit	Notes
Center Wavelength	λC	840	850	860	nm	
Data rate per lane	DR		25.78125		Gbps	
Optical Power for TX DISABLE				30	dBm	
Average launch power, each lane	Pavg	-8.4		2.4	dBm	
Optical Power OMA, each Lane	POMA	-6.4		3	dBm	
Extinction Ratio	ER	2			dB	
RMS spectral width	Δλ			0.6	nm	
Optical Return Loss Tolerance	ORLT			12	dB	

V. Receiver Optical Specifications

Parameter	Symbol	Min	Type	Max	Unit	Notes
Center Wavelength	λC	840	850	860	nm	
Data rate per lane	DR		25.78125		Gbps	
Overload input optical power	RH	2.4				

Stressed receiver sensitivity (OMA),each lane(5E-5)	Vin			-5.2	dBm	
Rx LOS Assert	Ts	-30			dBm	
Rx LOS De-assert	Vcc			-10	dBm	
Rx LOS Hysteresis	RH	0.5			dB	

VI. High Speed Electrical Specifications

Parameter	Min	Type	Max	Unit	Notes
Input differential impedance	90	100	110	Ω	
Differential data input swing	300	25.78125	1100	mV	
Differential data output swing	500		800	mV	
Input Logic Level High	2		Vcc	V	
Input Logic Level Low	0		0.8	V	
Output Logic Level High	Vcc-0.5		Vcc	V	
Output Logic Level Low	0		0.4	V	

VII. Wire Electrical Specifications

Parameter	Symbol	Min	Max	Unit
Host 2-wire Vcc voltage	Vcc_Host_2w	3.14	3.46	V

SCL and SDA Voltage	VOL	0	0.4	V
	VOH	Vcc_Host _2w-0.5	Vcc_Host_2w+0.3	V
	VIL		VccT*0.3	V
	VIH	VccT*0.7	VccT+0.5	V
Input current on the SCL and SDA	II	-10	10	mA

VIII.Wire Timing Specifications

Parameter	Symbol	Min	Max	Unit	Notes
Clock Frequency	fSCL	100	400	kHz	1
Clock Pulse Width Low	tLOW	1.3		us	
Clock Pulse Width High	tHIGH	0.6			
Time bus free before new transmission can start	tBUF	20		us	2
START Hold Time	tHD,STA	0.6		us	
START Set-up Time	tSU,STA	0.6		us	
Data In Hold Time	tHD, DAT	0		us	
Data In Set-up Time	tSU, DAT	0.1		us	
Input Rise Time (100kHz)	tR, 100		1000	ns	3
Input Rise Time (400kHz)	tR, 400		300	ns	3

Input Fall Time (100kHz)	tF, 100		300	ns	4
Input Fall Time (400kHz)	tF, 400		300	ns	4
STOP Set-up Time	tSU, STO	0.6			

Notes:

1. Module shall operate with fSCL up to 100 kHz without requiring clock stretching. The module may clock stretch with fSCL greater than 100 kHz and up to 400 kHz.
2. Between STOP and START and between ACK and ReSTART.
3. From (VIL,MAX-0.15) to (VIH,MIN+0.15).
4. From (VIH,MIN+0.15) to (VIL,MAX-0.15).

IX.Memory Specifications

Parameter	Symbol	Min	Max	Unit	Notes
Serial Interface Clock Holdoff "Clock Stretching"	T_clock_hold		500	us	1
Complete Single or Sequential Write up to 4 Byte	tWR		40	ms	
Complete Sequential Write of 5~8 Byte	tWR		80	ms	
Endurance (Write Cycles)		10k		cycles	

NOTE:

1.Maximum time the QSFP28 module may hold the SCL line low before continuing with a read or write operation.

X. Digital Diagnostics Monitor Accuracy

Parameter	Accuracy	Unit	Calibration
Temperature	±3	ºC	Internal
Voltage	±3	%	Internal
Tx Bias Current (Each Lane)	10	%	Internal

Tx Output Power (Each Lane)	±3	dB	Internal
Rx Power (Each Lane)	±3	dB	Internal

XI. Pin Definitions

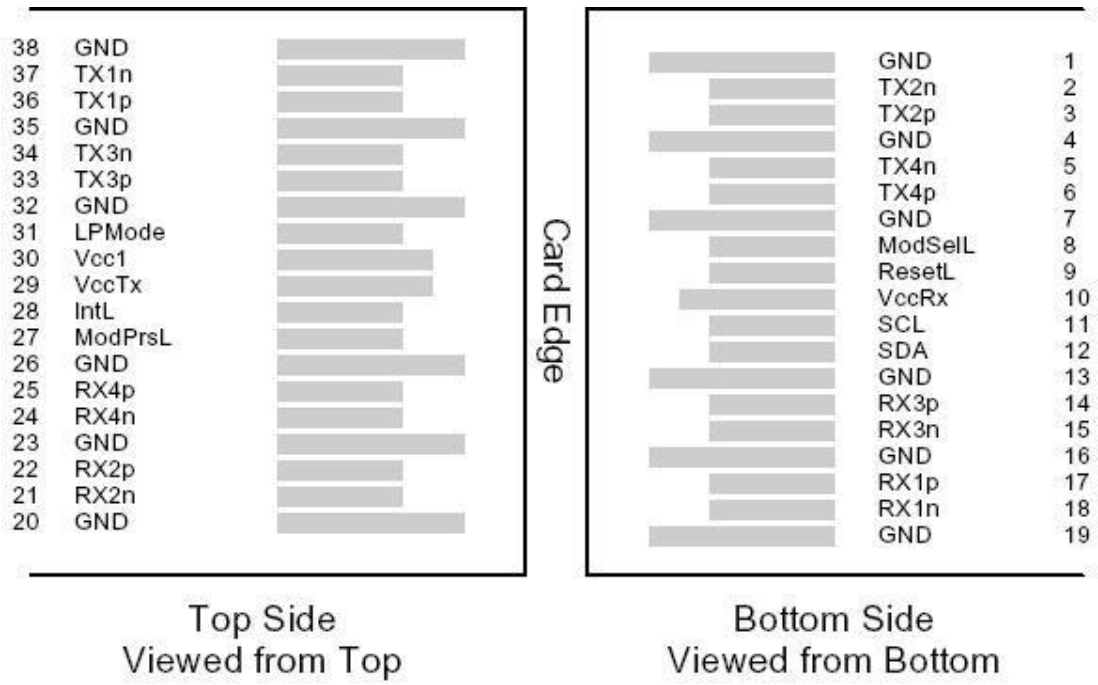


Figure 1 – QSFP28-compliant 38-pin connector (per SFF-8679)

Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3	
4		GND	Ground	1	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3	

7		GND	Ground	**1**	1
8	LVTTL-I	ModselL	Module Select	3	
9	LVTTL-I	ResetL	Module Reset	3	
10		Vcc Rx	+3.3V Power Supply Receiver	2	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3	
13		GND	Ground	1	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3	
15	CML-O	Rx3n	Receiver Inverted Data Output	3	
16		GND	Ground	1	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3	
18	CML-O	Rx1n	Receiver Inverted Data Output	3	
19		GND	Ground	1	1
20		GND	Ground	1	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3	
23		GND	Ground	1	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3	

25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3	
26		GND	Ground	1	1
27	LVTTL-O	ModPrsL	Module Present	3	
28	LVTTL-O	IntL	Interrupt	3	
29		Vcc Tx	+3.3V Power supply transmitter	2	2
30		Vcc1	+3.3V Power supply	2	2
31	LVTTL-I	LPMode	Low Power Mode	3	
32		GND	Ground	1	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3	
35		GND	Ground	1	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3	
38		GND	Ground	1	1

Note1:

GND is the symbol for signal and supply (power) common for the QSFP+ module. All are common within the QSFP+ module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

Note2:

Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently.

IV. Mechanical Specifications

The mechanical specifications are compliant to the QSFP28 transceiver module specifications.