100G/200G DWDM Tunable CFP2 DCO 50GHz 80km DOM LC SMF Transceiver

DWDM-200CFP2-DCO-LL

Applications

- The 100G / 200G CFP2-DCO coherent optical module is used on the host system for MAN DWDM applications.

Features

- 100G CFP2-DCO Coherent Optical Module 0perating up to 112.30 Gbps
- 200G CFP2-DCO Coherent Optical Module Operating up to 211.45 Gbps
- PM-QPSK (100G) and PM-16QAM (200G) Modulation Formats
- 100GE, OTU4, OTUC1 and OTUC2 Services
- Electrical Interfaces OTL4.4, OTLC1.4, CAU-I4, OTLC2.8 and CEI-28G-MR
- CFP2 MSA Hardware Specification 1.0 with Modifications Compliant
- CFP MSA Management Interface Specification 2.2 with Modifications Compliant
- Near-End / Remote-End Data Loopback
- Hot-Pluggable CFP2 Form Factor
- Maximum Power Consumption: 24 W

Description

The 100G / 200G CFP2-DCO coherent optical module is a high-performance, cost-effective transceiver which uses a 104-pin CFP2-MSA electrical connector for connecting the host card. The optical module consists of three functional parts: TX module, RX module and control module and has a LC optics interface and Digital diagnostics functions. They are compliant with IEEE 802.3, CFP2 MSA, CFP MSA.

Product Specifications

I. Performance Specifications

Parameter	Value
100G Optical Port	
Network Lane, Modulation Format	PM-QPSK
Optical Channels	96
Grid Spacing	50GHz
Frequency Range	191.3 to 196.05THz
Wavelength Stability	±1.5GHz
Tx Output Power, Default	-0.5dBm
Max. Tx Output Power	-0.5dBm
Min. Tx Output Power	-6.5dBm
Tx Output Power Accuracy	±1.5dBm
Output Power During Tuning	<-35dBm
CD Tolerance	±40000ps/nm
DGD Tolerance	50ps
Input Power Range	0to-18dBm
OSNR Tolerance (BOL)	12.5dB (Rx optical power: -8 to -10dBm)
Power Consumption	Typical: 22W Maximum: 24W

Parameter	Value
200G Optical Port	
Network Lane, Modulation Format	PM-16QAM
Optical Channels	96
Grid Spacing	50GHz
Frequency Range	191.3 to 196.05THz
Wavelength Stability	±1.5GHz
Tx Output Power, Default	-0.5dBm
Max. Output Optical Power	-0.5dBm
Min. Tx Output Power	-6.5dBm
Tx Output Power Accuracy	±1.5dBm
Output Power During Tuning	<-35dBm
CD Tolerance	±40000ps/nm
DGD Tolerance	22ps
Input Power Range	0to-18dBm
OSNR Tolerance (BOL)	18.5dB (Rx Optical Power: -8 to -10dBm)
Power Consumption	Typical: 22W Maximum: 24W

II. Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
Storage Temperature	-40	85	℃

Parameter	Min.	Max.	Unit
Operating Case Temperature	0	70	ºC
Relative Humidity, Operating (non-condensing)	5	85	%
Relative Humidity, Operating (Shortterm<96hrs, Non-Condensing)	5	95	%
ESD Sensitivity (HBM)		High-Speed Pins: 1000 Other Pins:2000	V

III. Electrical Characteristics

1. Power Supply Requirements

The 100G / 200G CFP2 coherent optical module is powered by an independent 3.3 V power supply on the host. All voltages are tested at the connector interfaces.

Parameter	Symbol	Min.	Typical	Max.	Unit	Note
3.3V DC Power Supply Voltage	V_{CC}	3.2	3.3	3.4	V	±5%
3.3V DC Power Supply Current	I_{CC}			7.3	A	Note1&2
Power Supply Noise	Vrip			2	%p-p	DC-1MHz
				3		1-10MHz
Power Consumption	Pw_class 4		22	24	W	200G Mode
Operating Temperature	T	0		70	ºC	

Note:

1. The Min. and Max. values apply to the full temperature range at the EOL of the module. Typical values (Typ.) are defined at the BOL of the module, with operating temperature at 25ºC and expected power supplied.
2. The maximum current of each pin cannot exceed 1.3 A.
3. The Max. value of Icc is for design reference, and the expected working current cannot exceed Pw_normal/Vcc.

2.High-Speed Electrical Interface Specifications

2.1 Transmitter Data (TX)

The transmitter data signal complies with the CEI-28G-MR low swing standards.

2.2 Receiver Data (RX)

The receiver data signal complies with the CEI-28G-MR standards.

2.3 Reference Clock (REFCLK)

The host does not need to provide a reference clock (REFCLK) for the 100G / 200G CFP2-DCO coherent optical module, because a 622.08M local clock is integrated in the 200G CFP2-DCO coherent optical module.

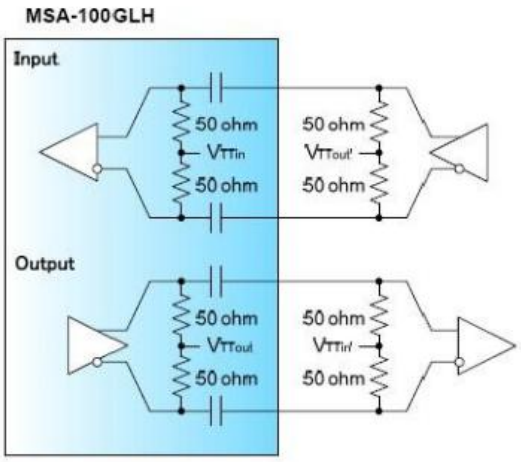

Figure 1. High-Speed I/O for Data and Clocks

2.4 Transmitter Monitor Clock (TXMCLK)

The transmitter of the 100G / 200G CFP2-DCO coherent optical module provides a monitoring clock TXMCLK, which is mainly used as a reference for monitoring optical signals at the transmitter. The clock can be used to trigger a high-speed sampling oscilloscope.

Parameter	Symbol	Min.	Typical	Max.	Unit	Note
Impedance	Zd	80	100	120	Ω	
Transmitter Monitor Clock Frequency (TXMCLK)			1/ 48		Hz	The Frequency is1/48 the Symbol Rate of the Transmitter's Optical Signal.
TXMCLK Differential Voltage	VDIFFTX	500		1000	mV	Differential Peak-to-Peak Voltage

3.Control Pins (non-MDIO) Functional Description

3.1 TX_DIS (Transmitter Disable)

TX_DIS is an input pin which receives signals from the host and operates in the logic high state. When TX_DIS is logic high, the output optical signal inside the optical module is turned off. When TX_DIS is logic low, the output optical signal inside the optical module is turned on. The symbol "t_on" is the turn-on time and "t_off" is the turn-off time. Figure 4-2 shows the timing diagram.

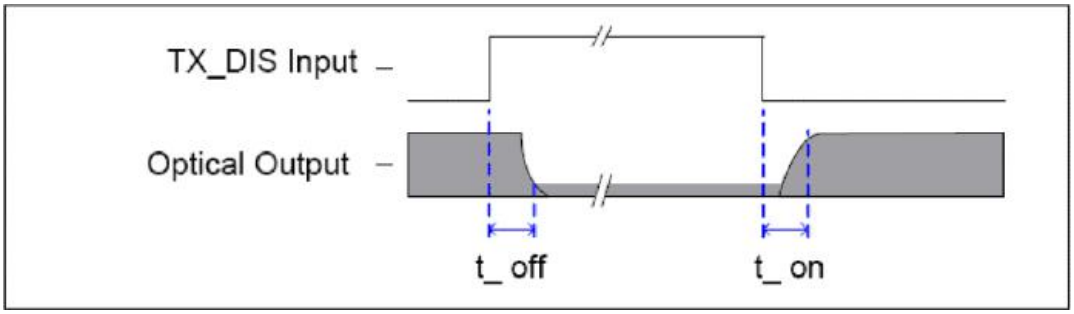

Figure 2. Timing Diagram for TX_DIS

3.2 MOD_LOPWR (Module Low Power)

MOD_LOPWR is an input pin which receives signals from the host and works in the logic high state. When MOD_LOPWR is logic high, the optical module works at low power consumption and remains in this mode. When MOD_LOPWR is pulled down, the optical module is initialized to a high power consumption state, that is, the normal operation mode. In low power consumption mode, the optical module communicates through the MDIO management interface, and its maximum power consumption does not exceed 2 W. Figure 4-3 shows the values of "t_MOD_LOPWR_on" and "t_ MOD_LOPWR_off".

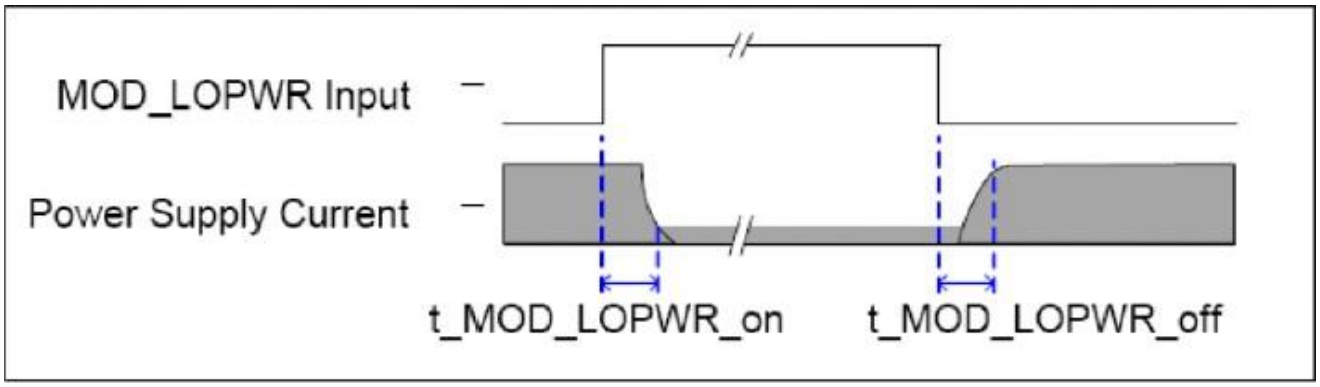

Figure 3. Timing Diagram for MOD_LOPWR

3.3 MOD_RSTn (Module Reset)

MOD_RSTn is an input pin which receives signals from the host and works in the logic low state. When MOD_RSTn is pulled low, the optical module is in the reset state. When MOD_RSTn is logic high, the optical module exits the reset mode and starts power-on initialization.

4. Alarm Pins (non-MDIO) Functional Description

4.1 RX_LOS (Receiver Loss of Signal)

RX_LOS is an output pin which transmits signals to the host and works at the logic high state. When RX_LOS is logic high, the optical power received by the optical module is too low. Figure 4-4 shows the timing diagram for RX_LOS.

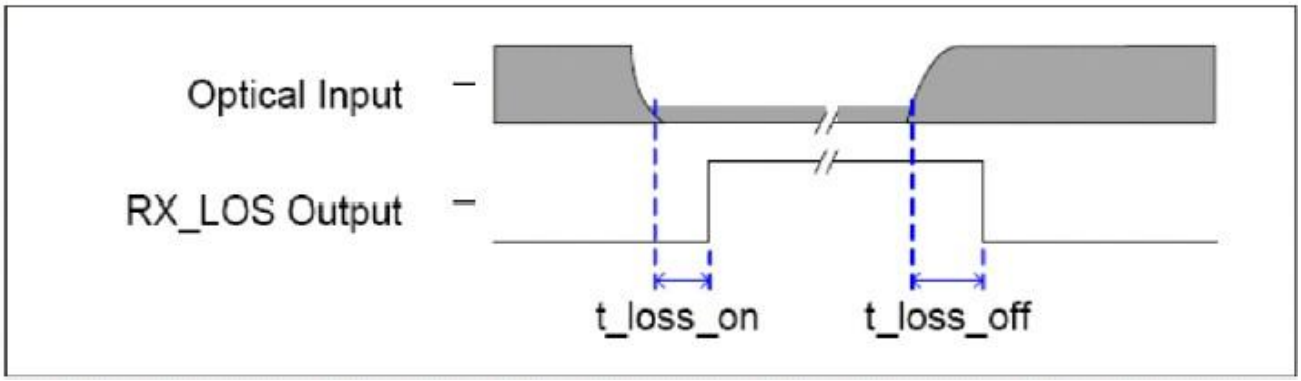

Figure 4. Timing Diagram for RX_LOS

4.2 MOD_ABS (Module Absent)

MOD_ABS is an output pin which transmits signals from the inside of the module to the host. This pin is pulled up on the host and pulled down to the ground inside the module. When the optical module is inserted into the host, MOD_ABS is logic low, meaning that the module is present. When the optical module is absent on the host, MOD_ABS is logic high, meaning that the module is absent.

5. Control and Alarm Descriptions

5.1 Timing Parameters for Control and Alarm Signals

Parameter	Symbol	Min.	Max.	Unit
Transmitter Disabled (TX_DIShigh)	t_off		1	ms
Transmitter Enabled(TX_DISlow)	t_on		25	s
MOD_LOPWR Assert	t_MOD_LOPWR_assert		25	s
MOD_LOPWR Deassert	t_MOD_LOPWR_deassert		25	s
Receiver Loss of Signal Assert Time	t_loss_on		1	ms
Receiver Loss of Signal De-assert Time	t_loss_off		15	ms
Initialization Time from Reset	t_initialize	190	220	s

5.2 V LVCMOS Electrical Characteristics

The 3.3 V LVCMOS level of the hardware control and alarm signal pins described above shall meet the electrical characteristics described in Table 4-6. Figure 4-5 shows the recommended input and output termination modes for these pins.

Parameter	Symbol	Min.	Typical	Max.	Unit
Power Supply Voltage	V_{CC}	3.2	3.3	3.4	V
Input High Voltage	VIH	2		VCC+0.3	V
Input Low Voltage	VIL	-0.3		0.8	V
Input Leakage Current	IIN	-10		10	μA
Output High Voltage (IOH=-100 μA)	VOH	V_{CC}-0.2			V
Output Low Voltage (IOL=100μA)	VOL			0.2	V

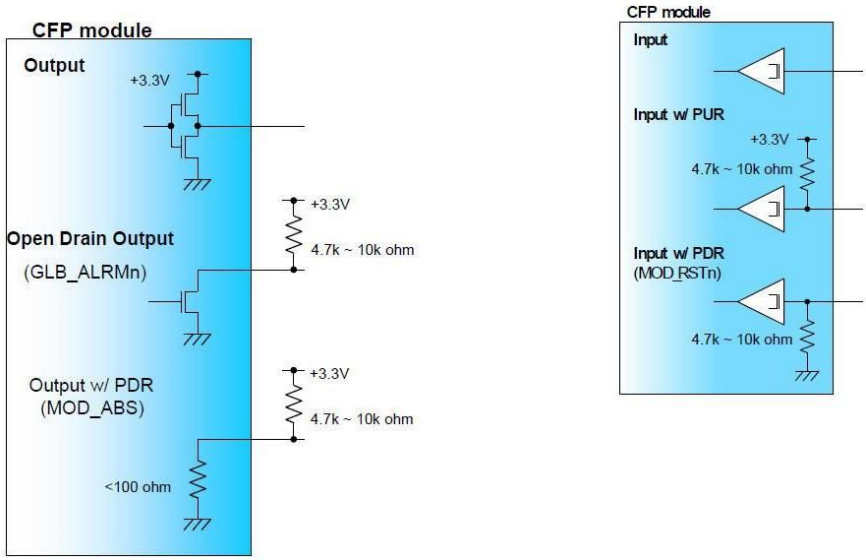

Figure 5. Reference 3.3 V LVCMOS Input / Output Termination

6. Module Management Interface Pins (MDIO) Description

6.1 Management Data Input / Output (MDIO) Interface

The MDIO implementation is defined in IEEE 802.3 clause 45. The optical module supports a lane rate of up to 4 Mb/s. The MDIO of the optical module uses the 1.2 V LVCMOS logic level.

6.2 Management Data Clock (MDC) Interface Pins

The host defines that the maximum MDC rate can reach 4 MHz, so the maximum MDC rate that the optical module supports can reach 4 MHz. Figure 4-6 shows the timing diagram for the MDIO and MDC pins. The optical module should follow the minimum setup time "tsetup" and hold time "thold" requirements of the MDIO port supplementary protocol.

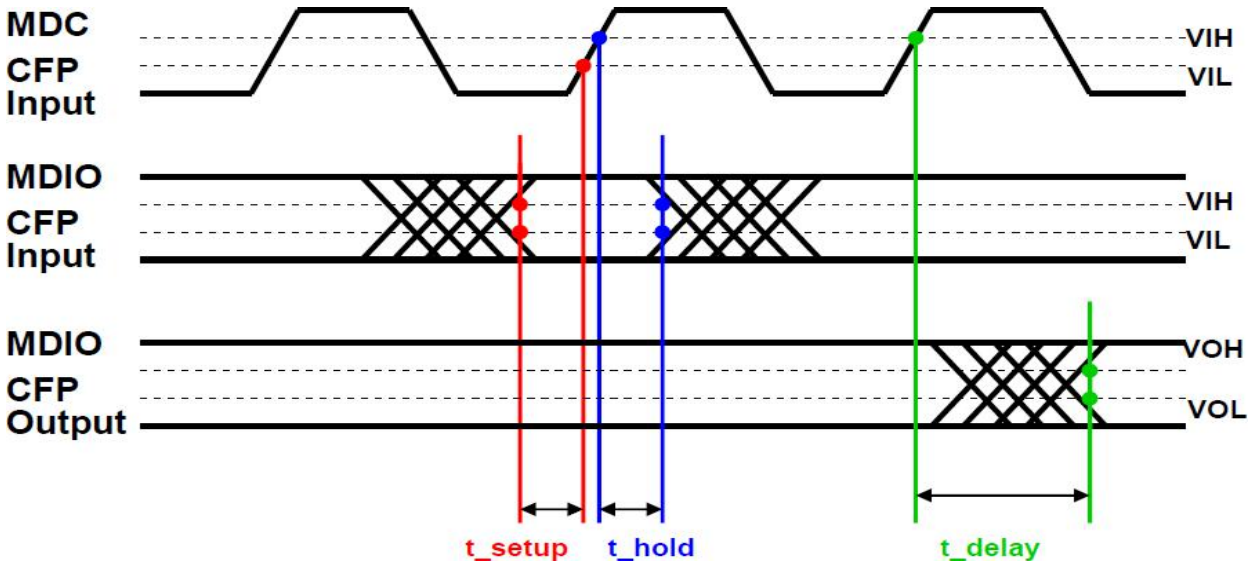

Figure 6. Timing Diagram for the MDIO & MDC Interfaces

6.3 MDIO Physical Port Address Pins (PRTADRs)

The PRTADRs are used by the host system to assign addresses to all optical modules belonging to its management area. PREADR0 corresponds to the LSB of the physical port address bit. The host drives the physical port address line of 5pin to set the physical port address of the optical module by following the address protocol of the MDIO port. It is recommended that these physical port addresses should not change when the optical module is powered on.

6.4 V LVCMOS Electrical Characteristics

Parameter	Symbol	Min.	Max.	Unit
Input High Voltage	VIH	0.84	1.5	V
Input Low Voltage	VIL	-0.3	0.36	V
Input Leakage Current	IIN	-100	100	µA
Output High Voltage (IOH=-100µA)	VOH	1	1.5	V
Output Low Voltage (IOL=100µA)	VOL	-0.3	0.2	V
Output High Current	IOH		-4	mA
Output Low Current	IOL	+4		mA
Input Capacitance	Ci		10	pF

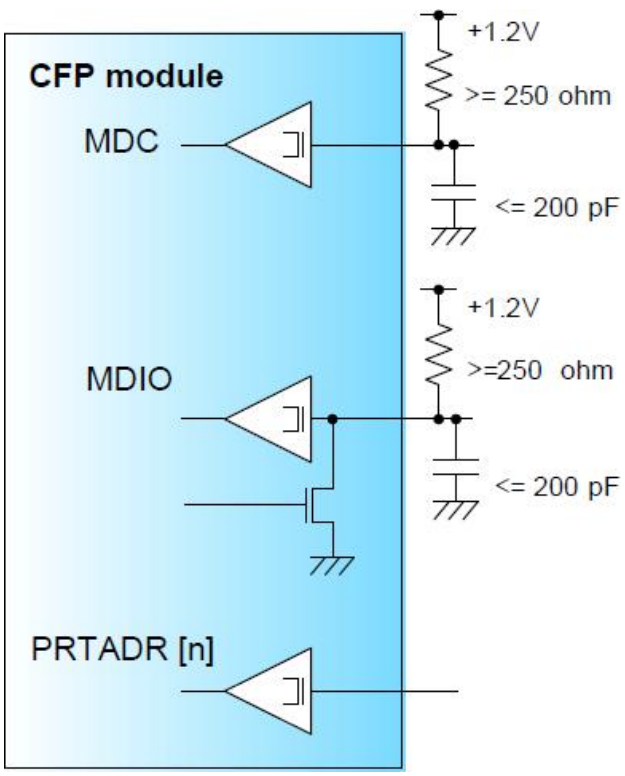

Figure 7. Reference MDIO Interface Termination

IV. Mechanical Specifications

the mechanical dimensions of the 100G / 200G CFP2-DCO coherent optical module. Max. dimensions (L × W × H): 107.5 mm × 42.5 mm × 13.4 mm

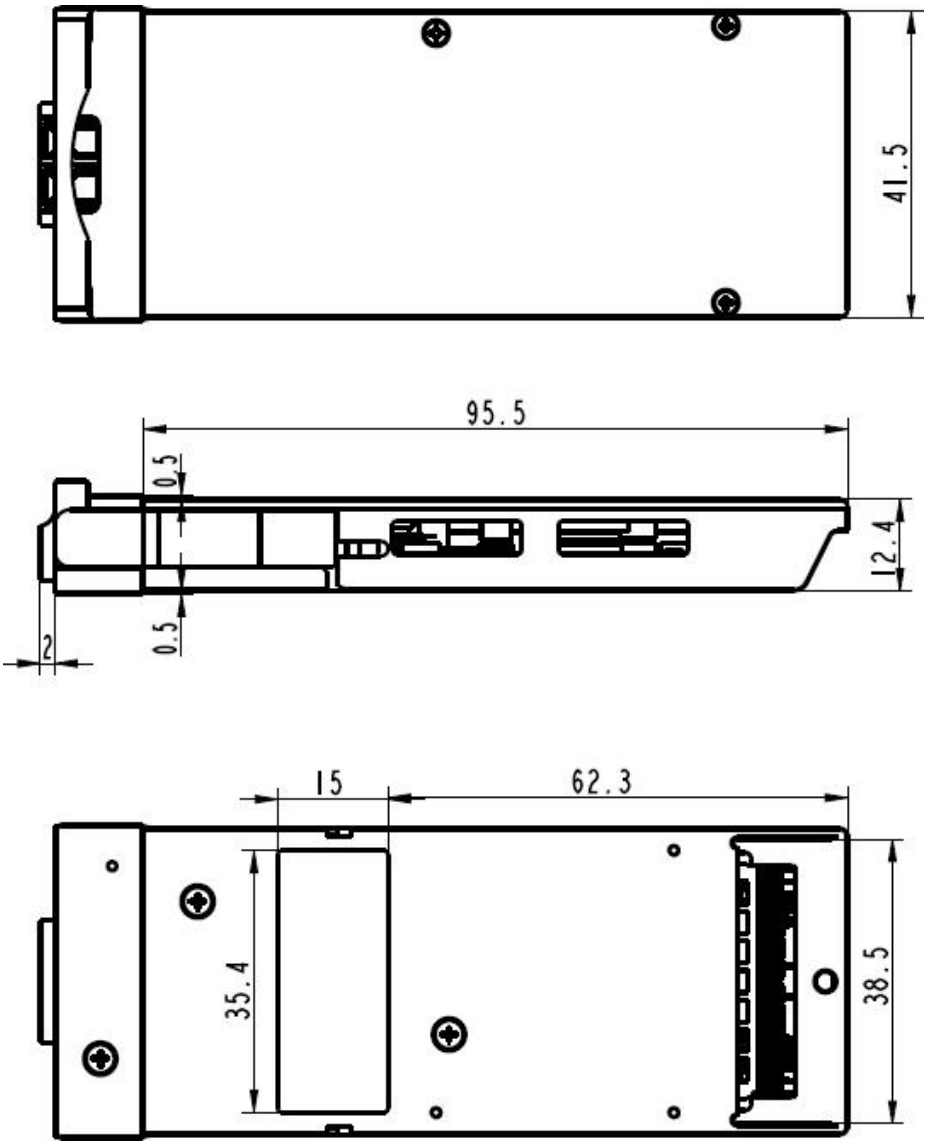

Figure 8. Mechanical Dimensions of the CFP2 Optical Module