

100GBASE-SR10 CXP 850nm 150m Transceiver Module

CXP-100GBASE-SR10-LL



Application

- 100GBASE-SR10 100G Ethernet
- Multiple 1G/2G/4G/8G/10G Fibre Channel
- Infiniband transmission at 12ch SDR, DDR and QDR
- Switches, Routers
- Data Centers
- Other 120G Interconnect Requirement

Features

- 12-channel full-duplex transceiver module
- Hot Pluggable CXP footprint
- Maximum link length of 300m on OM3 or 400m on OM4 Multimode Fiber (MMF)
- Multirate capability: 1.06Gb/s to 10.5Gb/s per channel
- Unretimed CPPI electrical interface
- Requires 3.3V power supply only
- Low power dissipation: <3.5W
- Reliable VCSEL array technology
- Built-in digital diagnostic functions
- Commercial operating case temperature range: 0° C to 70° C
- Single MPO connector receptacle
- RoHS-6 Compliant (lead-free)

Description

Longline’s CXP-SR10-100G transceiver modules is a high performance , low power consumption , long reach interconnect solution supporting 100G Ethernet, Infiniband QDR,DDR,SDR,1G/2G/4G/8G/10G fiber channel and PCIe. It is compliant with the 120Gbits Small Form factor Hot-Pluggable CXP-interface. Longline’s CXP transceiver modules is an assembly of 12 full-duplex lanes, where each lane is capable of transmitting data at rates up to 10.5Gb/s, providing an aggregated rate of 120Gb/s.

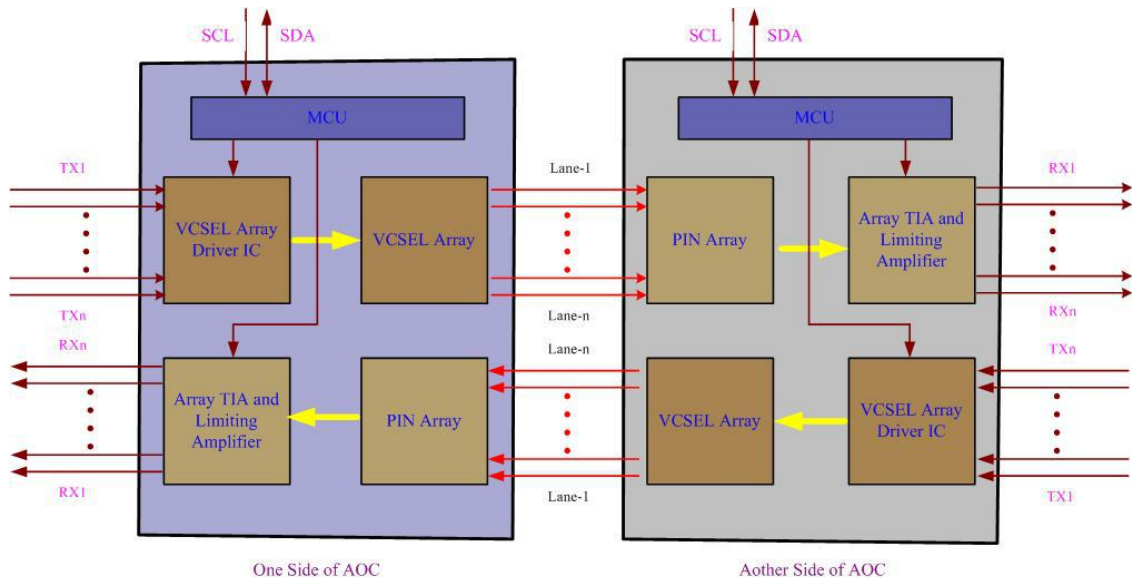


Figure1 - Module Block Diagram

Product Specifications

I. General Specifications

Parameter	Symbol	Min	Typ.	Max	Unit	Ref.
Differential input impedance	Z _{in}	90	100	110	ohm	
Differential Output impedance	Z _{out}	90	100	110	ohm	
Differential input voltage amplitude	ΔV _{in}	200		1200	mVp-p	
Differential output voltage amplitude	ΔV _{out}	600		800	mVp-p	
Skew	S _w			300	ps	
Bit Error Rate	BR			E-12		
Input Logic Level High	V _{IH}	2.0		VCC	V	
Input Logic Level Low	V _{IL}	0		0.8	V	
Output Logic Level High	V _{OH}	VCC-0.5		VCC	V	
Output Logic Level Low	V _{OL}	0		0.4	V	

Note:

1. BER=10⁻¹²; PRBS 2³¹-1@10.3125Gbps.
2. Differential input voltage amplitude is measured between TxnP and TxnN
3. Differential output voltage amplitude is measured between RxnP and RxnN.

II. Absolute Maximum Ratings

Parameter	Symbol	Min	Typ.	Max	Unit	Ref.
Supply Voltage	V _{cc}	-0.3		3.6	V	
Input Voltage	V _{in}	-0.3		V _{cc} +0.3	V	
Storage Temperature	T _{st}	-20		85	°C	
Case Operating Temperature	T _{op}	0		70	°C	
Humidity(non-condensing)	R _h	5		95	%	

III. Optical Characteristics (TOP = 0 to 70°C, VCC = 3.3 ± 5% Volts)

Parameter	Symbol	Min	Typ.	Max	Unit	Ref.
Transmitter (per Lane)						
Signaling Speed per Lane			10.5		GBd	1
Center wavelength		840		860	nm	
RMS Spectral Width	SW			0.65	nm	
Average Launch Power per Lane	TXP _x	-7.6		2.4	dBm	
Transmit OMA per Lane	TxOMA	-5.6		3.0	dBm	2
Difference in Power between any two lanes [OMA]	DP _x			4.0	dB	
Peak Power per Lane	PP _x			4.0	dBm	
Launch Power [OMA] minus TDP per Lane	P-TDP	-6.5			dBm	
TDP per Lane	TDP			3.5	dBm	
Optical Extinction Ratio	ER	3.0			dB	

Optical Return Loss Tolerance	ORL			12	dB	
Encircled Flux	FLX	> 86% at 19 um < 30% at 4.5 um			dBm	
Average launch power of OFF transmitter, per lane				-30	dBm	
Relative Intensity Noise	RIN			-128	dB/Hz	3
Transmitter eye mask definition {X1, X2, X3, Y1, Y2, Y3}		0.23, 0.34, 0.43, 0.27, 0.35, 0.4				

Receiver

Signaling Speed per Lane			10.5		GBd	4
Center wavelength		840		860	nm	
Damage Threshold	DT	3.4			dBm	
Average Receive Power per Lane	RXPx	-9.5		2.4	dBm	
Receive Power (OMA) per Lane	RxOMA			3.0	dBm	
Stressed Receiver Sensitivity (OMA) per Lane	SRS			-5.4	dBm	
Peak Power, per lane	PPx			4	dBm	
Receiver Reflectance	Rfl			-12	dB	
Vertical eye closure penalty, per lane				1.9	dB	
Stressed eye J2 jitter, per Lane				0.3	UI	

Stressed eye J9 jitter, per Lane				0.47	UI	
OMA of each aggressor lane				-0.4	dBm	
Receiver jitter tolerance [OMA], per Lane				-5.4	dBm	
Rx jitter tolerance: Jitter frequency		(75, 5)			kHz, UI	
and p-p amplitude		(375, 1)			kHz, UI	
LOS De-Assert	LOSD			-11	dBm	
LOS Assert	LOSA			-14	dBm	
LOS Hysteresis		1			dB	

IV. Electrical Characteristics (TOP = 0 to 70°C, VCC = 3.3 ± 5% Volts)

NOTE: The CXP-SR10-100G requires that a CPPI-compliant CXP electrical connector be used on the host board in order to guarantee its electrical interface specification. Please check with your connector supplier.

Parameter	Symbol	Min	Typ.	Max	Unit	Ref.
Supply Voltag	Vcc1, VccTx, VccRx	3.15	3.3	3.45	V	
Supply Current	Icc	950		1050	mA	
Module Total Power	P			3.5	W	1
Link Turn-On Time						
Transmit turn-on time				2000	ms	2
Transmitter (per Lane)						
Single ended input voltage tolerance	VinT	-0.3		4.0	V	
Differential data input swing	Vin,pp	120		1200	mVpp	3
Differential input threshold			50		mV	
AC common mode input voltage tolerance (RMS)		15			mV	
Differential input return loss		Per IEEE 802.3ba, Section 86A.4.1.1			dB	4
J2 Jitter Tolerance	Jt2	0.17			UI	
J9 Jitter Tolerance	Jt9	0.29			UI	
Data Dependent Pulse Width Shrinkage	DDPWS	0.07			UI	
Eye mask coordinates {X1, X2 Y1, Y2}			0.11, 0.31 95, 350		UI mV	5
Receiver (per Lane)						
Single-ended output voltage		-0.3		4.0	V	
Differential data output swing	Vout,pp	0		800	mVpp	6.7

AC common mode output voltage (RMS)				7.5	mV	
Termination mismatch at 1 MHz				5	%	
Differential output return loss			Per IEEE 802.3ba, Section 86A.4.2.1		dB	4
Common mode output return loss			Per IEEE 802.3ba, Section 86A.4.2.2		dB	4
Output transition time, 20% to 80%		28			ps	
J2 Jitter output	Jo2	0.42			UI	
J9 Jitter output	Jo9	0.65			UI	
Eye mask coordinates {X1, X2 Y1, Y2}			0.29, 0.5 150, 425		UI mV	5
Power Supply Ripple Tolerance	PSR	50			mVpp	

Notes:

1. Maximum total power value is specified across the full temperature and voltage range.
2. From power-on and end of any fault conditions.
3. After internal AC coupling. Self-biasing 100 Ohm differential input.
4. 10 MHz to 11.1 GHz range
5. Hit ratio = 5×10^{-5}
6. AC coupled with 100 Ohm differential output impedance.
7. Settable in 4 discrete steps via the I2C interface. See Figure 2 for Vout settings.

V. Pin Descriptions

Receiver -- Top Card			
C1	GND		D1
C2		Rx1p	D2
C3		Rx1n	D3
C4	GND		D4
C5		Rx3p	D5
C6		Rx3n	D6
C7	GND		D7
C8		Rx5p	D8
C9		Rx5n	D9
C10	GND		D10
C11		Rx7p	D11
C12		Rx7n	D12
C13	GND		D13
C14		Rx9p	D14
C15		Rx9n	D15
C16	GND		D16
C17		Rx11p	D17
C18		Rx11n	D18
C19	GND		D19
C20		PRSENT_L	D20
C21		Int_L/Reset_L	D21

Card Edge

Transmitter -- Bottom Card

A1	GND		B1
A2		Tx1p	B2
A3		Tx1n	B3
A4	GND		B4
A5		Tx3p	B5
A6		Tx3n	B6
A7	GND		B7
A8		Tx5p	B8
A9		Tx5n	B9
A10	GND		B10
A11		Tx7p	B11
A12		Tx7n	B12
A13	GND		B13
A14		Tx9p	B14
A15		Tx9n	B15
A16	GND		B16
A17		Tx11p	B17
A18		Tx11n	B18
A19	GND		B19
A20		SCL	B20
A21		SDA	B21

Card Edge

Figure2- Electrical Pin-out Details

Pin	Logic	Symbol	Name/Description	Ref.
A1		GND	Module Ground	1
A2	CML-I	Tx1+	Transmitter non-inverted data input	
A3	CML-I	Tx1-	Transmitter inverted data input	
A4		GND	Module Ground	1
A5	CML-I	Tx3+	Transmitter non-inverted data input	
A6	CML-I	Tx3-	Transmitter inverted data input	
A7		GND	Module Ground	1
A8	CML-I	Tx5+	Transmitter non-inverted data input	
A9	CML-I	Tx5-	Transmitter inverted data input	
A10		GND	Module Ground	1
A11	CML-I	Tx7+	Transmitter non-inverted data input	
A12	CML-I	Tx7-	Transmitter inverted data input	
A13		GND	Module Ground	1
A14	CML-I	Tx9+	Transmitter non-inverted data input	
A15	CML-I	Tx9-	Transmitter inverted data input	
A16		GND	Module Ground	1
A17	CML-I	Tx11+	Transmitter non-inverted data input	
A18	CML-I	Tx11-	Transmitter inverted data input	
A19		GND	Module Ground	1

A20	LVC MOS-I	SCL	2-wire Serial interface clock	2
A21	LVC MOS-I/O	SDA	2-wire Serial interface data	2
B1		GND	Module Ground	1
B2	CML-I	Tx0+	Transmitter non-inverted data input	
B3	CML-I	Tx0-	Transmitter inverted data input	
B4		GND	Module Ground	1
B5	CML-I	Tx2+	Transmitter non-inverted data input	
B6	CML-I	Tx2-	Transmitter inverted data input	
B7		GND	Module Ground	1
B8	CML-I	Tx4+	Transmitter non-inverted data input	
B9	CML-I	Tx4-	Transmitter inverted data input	
B10		GND	Module Ground	1
B11	CML-I	Tx6+	Transmitter non-inverted data input	
B12	CML-I	Tx6-	Transmitter inverted data input	
B13		GND	Module Ground	1
B14	CML-I	Tx8+	Transmitter non-inverted data input	
B15	CML-I	Tx8-	Transmitter inverted data input	
B16		GND	Module Ground	1
B17	CML-I	Tx10+	Transmitter non-inverted data input	1
B18	CML-I	Tx10-	Transmitter inverted data input	
B19		GND	Module Ground	1

B20		VCC3.3-TX	+3.3v Transmitter Power Supply	
B21		VCC12-TX	+12v Transmitter Power Supply, Unconnected	
C1		GND	Module Ground	1
C2	CML-O	RX1+	Receiver non-inverted data output	
C3	CML-O	RX1-	Receiver inverted data output	
C4		GND	Module Ground	1
C5	CML-O	RX3+	Receiver non-inverted data output	
C6	CML-O	RX3-	Receiver inverted data output	
C7		GND	Module Ground	1
C8	CML-O	RX5+	Receiver non-inverted data output	
C9	CML-O	RX5-	Receiver inverted data output	
C10		GND	Module Ground	1
C11	CML-O	RX7+	Receiver non-inverted data output	
C12	CML-O	RX7-	Receiver inverted data output	
C13		GND	Module Ground	1
C14	CML-O	RX9+	Receiver non-inverted data output	
C15	CML-O	RX9-	Receiver inverted data output	
C16		GND	Module Ground	1
C17	CML-O	RX11+	Receiver non-inverted data output	
C18	CML-O	RX11-	Receiver inverted data output	
C19		GND	Module Ground	1

C20	LVTTTL-O	PRSNT_L	Module Present, pulled down to GND	
C21	LVTTTL-I/O	INT_L/Reset_L	Interrupt output, Module Reset	2
D1		GND	Module Ground	1
D2	CML-O	RX0+	Receiver non-inverted data output	
D3	CML-O	RX0-	Receiver inverted data output	
D4		GND	Module Ground	1
D5	CML-O	RX2+	Receiver non-inverted data output	
D6	CML-O	RX2-	Receiver inverted data output	
D7		GND	Module Ground	1
D8	CML-O	RX4+	Receiver non-inverted data output	
D9	CML-O	RX4-	Receiver inverted data output	
D10		GND	Module Ground	1
D11	CML-O	RX6+	Receiver non-inverted data output	
D12	CML-O	RX6-	Receiver inverted data output	
D13		GND	Module Ground	1
D14	CML-O	RX8+	Receiver non-inverted data output	
D15	CML-O	RX8-	Receiver inverted data output	
D16		GND	Module Ground	1
D17	CML-O	RX10+	Receiver non-inverted data output	
D18	CML-O	RX10-	Receiver inverted data output	
D19		GND	Module Ground	1

D20	VCC3.3-RX	+3.3v Receiver Power Supply
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D21 VCC12-RX +12v Receiver Power Supply, Unconnected

Notes:

1. Module circuit ground is isolated from module chassis ground within the module.
2. Open collector; should be pulled up with 4.7k – 10k ohms on host board to a voltage between 3.15V and 3.6V.

VI. Mechanical Specifications

