longline

# 100GBASE-PSM4 QSFP28 1310nm 500m DOM Transceiver

CPAC-TR-100PIR-SSM160-QSFP28-C-LL



#### Application

- 100G Ethernet links
- Infiniband QDR and DDR interconnects
- Datacenter and Enterprise networking

#### Features

- 4 independent full-duplex channels
- Up to 28Gb/s data rate per channel
- QSFP28 MSA compliant
- Compliant to IEEE 802.3bm 100GBASE PSM4
- Up to 500m reach for G.652 SMF
- Maximum power consumption 3.5W
- Single +3.3V power supply
- Operating case temperature: 0 to 70°C
- RoHS-6 compliant

#### **General Description**

This product is a parallel 100Gb/s Quad Small Form-factor Pluggable (QSFP28) optical module. It provides increased port density and total system cost savings. The QSFP28 full-duplex optical module offers 4 independent transmit and receive channels, each capable of 25Gb/s operation for an aggregate data rate of 100Gb/s on 2km of single mode fiber.

An optical fiber ribbon cable with an MTP/MPO connector can be plugged into the QSFP28 module receptacle. Proper alignment is ensured by the guide pins inside the receptacle. The cable usually cannot be twisted for proper channel to channel alignment. Electrical connection is achieved through an MSA-compliant 38-pin edge type connector.

The module operates with single +3.3V power supply. LVCMOS/LVTTL global control signals, such as Module Present, Reset, Interrupt and Low Power Mode, are available with the modules. A 2-wire serial interface is available to send and receive more complex control signals, and to receive digital diagnostic information. Individual channels can be addressed and unused channels can be shut down for maximum design flexibility.

The product is designed with form factor, optical/electrical connection and digital diagnostic interface according to the QSFP28 Multi-Source Agreement (MSA). It has been designed to meet the harshest external operating conditions including temperature, humidity and

EMI interference. The module can be managed through the I2C two-wire serial interface .

#### **Functional Description**

This product is a QSFP28 parallel single mode optical transceiver with an MTP/MPO fiber ribbon connector. The transmitter module accepts electrical input signals compatible with Common Mode Logic (CML) levels. All input data signals are differential and internally terminated. The receiver module converts parallel optical input signals via a photo detector array into parallel electrical output signals. The receiver module outputs electrical signals are also voltage compatible with Common Mode Logic (CML) levels. All data signals are differential and support a data rates up to 25Gb/s per channel. Figure 1 shows the functional block diagram of this product.

A single +3.3V power supply is required to power up the module. Both power supply pins VccTx and VccRx are internally connected and should be applied concurrently. Per MSA the module offers 7 low speed hardware control pins (including the 2-wire serial interface): ModSelL, SCL, SDA, ResetL, LPMode, ModPrsL and IntL.

Module Select (ModSelL) is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP28 modules on a single 2-wire interface bus – individual ModSelL lines for each QSFP28 module must be used.

Serial Clock (SCL) and Serial Data (SDA) are required for the 2-wire serial bus communication interface and enable the host to access the QSFP28 memory map.

The ResetL pin enables a complete module reset, returning module settings to their default state, when a low level on the ResetL pin is held for longer than the minimum pulse length. During the execution of a reset the host shall disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by posting an IntL (Interrupt) signal with the Data\_Not\_Ready bit negated in the memory map. Note that on power up (including hot insertion) the module should post this completion of reset interrupt without requiring a reset

Low Power Mode (LPMode) pin is used to set the maximum power consumption for the module in order to protect hosts that are not capable of cooling higher power modules, should such modules be accidentally inserted.

Module Present (ModPrsL) is a signal local to the host board which, in the absence of a module, is normally pulled up to the host Vcc. When a module is inserted into the connector, it completes the path to ground through a resistor on the host board and asserts the signal. ModPrsL then indicates a module is present by setting ModPrsL to a "Low" state.

Interrupt (IntL) is an output pin. Low indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL pin is an open collector output and must be pulled to the Host Vcc voltage on the Host board.

#### **Product Specifications**

#### I. Absolute Maximum Ratings

It has to be noted that the operation in excess of any absolute maximum ratings might cause permanent damage to this module.

Parameter	Symbol	Min	Max	Units	Notes
Storage Temperature	Ts	-40	85	degC	
Operating Case Temperature	T <sub>OP</sub>	0	70	degC	
Power Supply Voltage	V <sub>cc</sub>	-0.5	3.6	V	
Relative Humidity (non-condensation)	RH	0	85	%	
Damage Threshold, each Lane	TH <sub>d</sub>	4.5		dBm	

### **II. Electrical Characteristics**

The following electrical characteristics are defined over the Recommended Operating Environment unless otherwise specified.

Parameter	Symbol	Min	Typical	Мах	Units	Notes	
Power Consumption				3.5	W		
Supply Current	lcc			1.1	А		
Transceiver Power-on Initialization Time				2000	ms	1	
Transmitter (each Lane)							
Single-ended Input Voltage Tolerance (Note 2)		-0.3		4.0	V	Referred to TP1 signal common	
AC Common Mode Input		15			mV	RMS	

AC common mode input		15			mV	RMS
Voltage Tolerance		15			IIIV	NINS
Differential Input Voltage Swing Threshold		50			mVpp	LOSA Threshold
-						
Differential Input Voltage Swing	Vin,pp	190		700	mVpp	
Differential Input Impedance	Zin	90	100	110	Ohm	

#### **Receiver (each Lane)**

Single-ended Output Voltage		-0.3		4.0	V	Referred to signal common
AC Common Mode Output Voltage				7.5	mV	RMS
Differential Output Voltage Swing		300		850	mVpp	
Differential Output Impedance	Zout	90	100	110	Ohm	

#### Notes:

1. Power-on Initialization Time is the time from when the power supply voltages reach and remain above the minimum recommended operating supply voltages to the time when the module is fully functional.

2. The single ended input voltage tolerance is the allowable range of the instantaneous input signals.

## **III. Optical Characteristics**

All parameters are specified under the recommended operating conditions with PRBS31 data pattern unless otherwise specified.

Parameter	Symbol	Min	Typical	Мах	Units	Notes
		Transmitter				
Center Wavelength	$\lambda_{C}$	1295	1310	1325	nm	
Side Mode Suppression Ratio	SMSR	30			dB	
Total Average Launch Power	P <sub>T</sub>			8.0	dBm	
Average Launch Power, each Lane	$P_{AVG}$	-9.4		2.0	dBm	
Optical Modulation Amplitude (OMA), each Lane	P <sub>OMA</sub>	-3.5		2.2	dBm	1
Difference in Launch Power between any Two Lanes (OMA)	Ptx,diff			5	dB	
Launch Power in OMA minus Transmitter and Dispersion Penalty (TDP), each Lane		-4.3			dBm	
TDP, each Lane	TDP			2.9	dB	
Extinction Ratio	ER	3.5			dB	
Relative Intensity Noise	RIN			-128	dB/Hz	
Optical Return Loss Tolerance	TOL			20	dB	
Transmitter Reflectance	R <sub>T</sub>			-12	dB	
Average Launch Power OFF Transmitter, each Lane	Poff			-30	dBm	
Transmitter Eye Mask Definition {X1, X2, X3, Y1, Y2, Y3}		{0.31, C	).4, 0.45, 0.34, 0.	38, 0.4}		2

		Receiver				
Center Wavelength	$\lambda_{C}$	1295	1310	1325	nm	
Damage Threshold, each Lane	TH <sub>d</sub>	4.5			dBm	3
Average Receive Power, each Lane		-12.66		2.0	dBm	
Receive Power (OMA), each Lane				2.2	dBm	
Receiver Sensitivity (OMA), each Lane	SEN1			-9.0	dBm	4
Receiver Sensitivity (OMA), each Lane	SEN2			-12.0	dBm	5
Receiver Reflectance	R <sub>R</sub>			-26	dB	
Difference in Receive Power between any Two Lanes (OMA)	Prx,diff			5.5	dB	
LOS Assert	LOSA		-20		dBm	
LOS Deassert	LOSD		-18		dBm	
LOS Hysteresis	LOSH	0.5			dB	
Receiver Electrical 3 dB upper Cutoff Frequency, each Lane	Fc			31	GHz	

#### Notes:

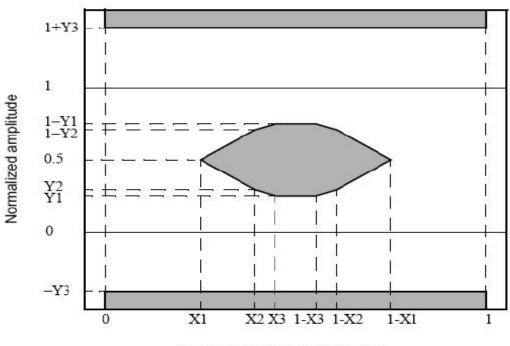
1. Even if the TDP < 0.8 dB, the OMA min must exceed the minimum value specified here.

2.See Figure 4 below.

3. The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operate correctly at this input power.

4. Measured at receiver input for  $BER = 1 \times 10^{-12}$ .

5. Measured at receiver input for  $BER = 5 \times 10^{-5}$ .



Normalized time (Unit Interval)

Figure 1. Eye Mask Definition

## **IV. Digital Diagnostic Functions**

The following digital diagnostic characteristics are defined over the normal operating conditions unless otherwise specified.

Parameter	Symbol	Min	Max	Units	Notes
Temperature monitor absolute error	DMI_Temp	-3	3	degC	Over operating temperature range
Supply voltage monitor absolute error	DMI_VCC	-0.1	0.1	V	Over full operating range
Channel RX power monitor absolute error	DMI_RX_Ch	-2	2	dB	1
Channel Bias current monitor	DMI_Ibias_Ch	-10%	10%	mA	
Channel TX power monitor absolute error	DMI_TX_Ch	-2	2	dB	1

#### Notes:

1. Due to measurement accuracy of different single mode fibers, there could be an additional +/-1 dB fluctuation, or a +/- 3 dB total accuracy.

#### V. Recommended Operating Conditions and Power Supply Requirements

Parameter	Symbol	Min	Typical	Max	Units
Operating Case Temperature	T <sub>OP</sub>	0		70	degC
Power Supply Voltage	V <sub>cc</sub>	3.135	3.3	3.465	V
Data Rate, each Lane			25.78125		Gb/s
Control Input Voltage High		2		Vcc	V
Control Input Voltage Low		0		0.8	V
Link Distance with G.652	D	0.002		2	km

## VI. Transceiver Block Diagram

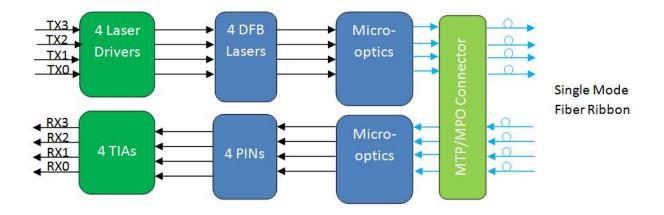


Figure 2. Transceiver Block Diagram

## VII. Pin Assignment and Description

38	GND		GND	1
37	TX1n		TX2n	
36	TX1p		TX2p	2
35	GND		GND	4
34	TX3n		TX4n	
33	TX3p		TX4p	6
32	GND		GND	2 3 5 6 7 eIL 8 L 9
31	LPMode	Card	ModS	୍ୟା ହ
30	Vcc1	Ω	5.4 C 1 1 1 1 2 1 1 1 2 1 1 2 1 2 1 2 1 2 1	
29	VccTx	a	Reset	
28	IntL	Edge	VccRx	
27	ModPrsL	<u>a</u>	SCL	11
26	GND	Q	SDA	12
25	RX4p	U U	GND	13
24	RX4n		RX3p	14
23	GND		RX3n	15
22	RX2p		GND	16
21	RX2n		RX1p	17
20	GND		RX1n	18
20	OND	- 2	GND	19

Top Side Viewed from Top Bottom Side Viewed from Bottom

#### Figure 3. QSFP28 Transceiver Electrical Connector Layout

#### **Pin Definition**

PIN	Logic	Symbol	Name/Description	Notes
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data output	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	
6	CML-I	Tx4p	Transmitter Non-Inverted Data output	
7		GND	Ground	1
8	LVTLL-I	ModSelL	Module Select	
9	LVTLL-I	ResetL	Module Reset	
10		VccRx	+3.3V Power Supply Receiver	2

## longline

12LVCMOS-I/OSDA2-Wire Serial Interface Data13GNDGround14CML-ORx3pReceiver Non-Inverted Data Output15CML-ORx3nReceiver Inverted Data Output16GNDGroundI17CML-ORx1pReceiver Non-Inverted Data Output18CML-ORx1pReceiver Inverted Data Output19GNDGNDGround20GNDGNDGround21CML-ORx2pReceiver Inverted Data Output22CML-ORx2pGround23GNDGroundI24CML-ORx4pReceiver Inverted Data Output	1
14CML-ORx3pReceiver Non-Inverted Data Output15CML-ORx3nReceiver Inverted Data Output16GNDGNDGround17CML-ORx1pReceiver Non-Inverted Data Output18CML-ORx1nReceiver Inverted Data Output19GNDGNDGround20GNDGNDGround21CML-ORx2nReceiver Inverted Data Output22CML-ORx2pReceiver Inverted Data Output23GNDGroundGround24CML-ORx4nReceiver Inverted Data Output	1
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16GNDGroundGround17CML-ORx1pReceiver Non-Inverted Data Output18CML-ORx1nReceiver Inverted Data Output19GNDGNDGround20GNDGRODGround21CML-ORx2nReceiver Inverted Data Output22CML-ORx2nGround23GNDGroundGround24CML-ORx4nReceiver Inverted Data Output	1
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18CML-ORx1nReceiver Inverted Data Output19GNDGround20GNDGround21CML-ORx2nReceiver Inverted Data Output22CML-ORx2pReceiver Non-Inverted Data Output23GNDGNDGround24CML-ORx4nReceiver Inverted Data Output	
19GNDGround20GNDGround21CML-ORx2n22CML-ORx2p33GNDGround24CML-ORx4n	
20GNDGround21CML-ORx2nReceiver Inverted Data Output22CML-ORx2pReceiver Non-Inverted Data Output23GNDGround24CML-ORx4nReceiver Inverted Data Output	
21CML-ORx2nReceiver Inverted Data Output22CML-ORx2pReceiver Non-Inverted Data Output23GNDGround24CML-ORx4nReceiver Inverted Data Output	1
22CML-ORx2pReceiver Non-Inverted Data Output23GNDGround24CML-ORx4nReceiver Inverted Data Output	
23GNDGround24CML-ORx4nReceiver Inverted Data Output	
24 CML-O Rx4n Receiver Inverted Data Output	
	1
25 CML-O Ry/n Deceiver Non-Inverted Data Output	1
25 CML-O Rx4p Receiver Non-Inverted Data Output	
26 GND Ground	1
27 LVTTL-O ModPrsL Module Present	
28 LVTTL-O IntL Interrupt	
29 VccTx +3.3 V Power Supply transmitter	2
30 Vcc1 +3.3 V Power Supply	2
31 LVTTL-I LPMode Low Power Mode	
32 GND Ground	1
33 CML-I Tx3p Transmitter Non-Inverted Data Input	
34 CML-I Tx3n Transmitter Inverted Data Output	
35 GND Ground	1
36 CML-I Tx1p Transmitter Non-Inverted Data Input	
37 CML-I Tx1n Transmitter Inverted Data Output	
38 GND Ground	

#### Notes:

- 1. GND is the symbol for signal and supply (power) common for QSFP28 modules. All are common within the QSFP28 module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground plane.
- 2. VccRx, Vcc1 and VccTx are the receiver and transmitter power suppliers and shall be applied concurrently. Recommended host board power supply filtering is shown in Figure 3 below. Vcc Rx, Vcc1 and VccTx may be internally connected within the QSFP28 transceiver module in any combination. The connector pins are each rated for a maximum current of 1000mA.

#### **VIII. Recommended Power Supply Filter**

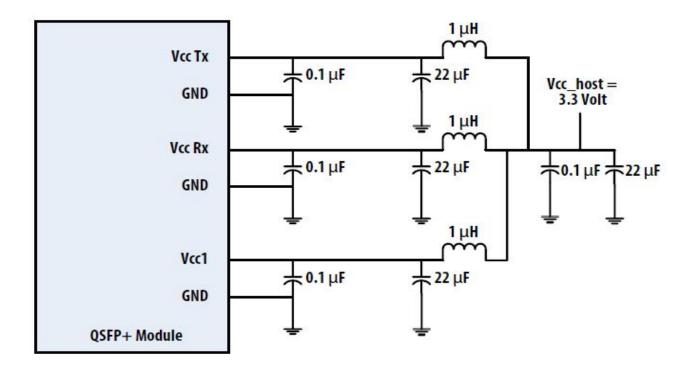
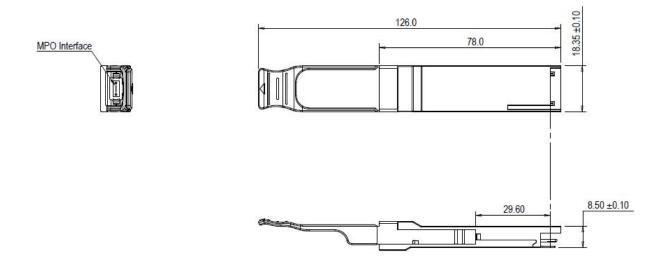


Figure 4. Recommended Power Supply Filter

#### **XI. Mechanical Dimensions**



#### Figure 5. Mechanical Outline

Attention: To minimize MPO connection induced reflections, an MPO receptacle with 8-degree angled end-face is utilized for this product. A female MPO connector with 8-degree end-face should be used with this product as illustrated in Figure 6.

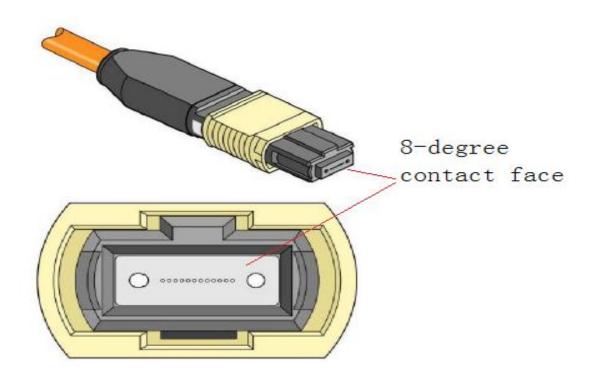


Figure 6. Female MPO Connector with 8-degree End-face

#### X. ESD

This transceiver is specified as ESD threshold 1KV for high speed data pins and 2KV for all others electrical input pins, tested per MIL-STD-883, Method 3015.4 /JESD22-A114-A (HBM). However, normal ESD precautions are still required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and handled only in an ESD protected environment.

## XI. Laser Safety

This is a Class 1 Laser Product according to EN 60825-1:2014. This product complies with 21 CFR 1040.10 and 1040.11 except for deviations pursuant to Laser Notice No. 50, dated (June 24, 2007).

Caution: Use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.