CFP2 100GBASE-LR4 1310nm 10km Transceiver Module

CFP2-100GBASE-LR4-LL

Application

- 100GE Routers and Switches
- 100G OTN
- 100G Network Security And Monitoring

Features

- Hot Pluggable CFP2 MSA package
- IEEE 802.3ba 100GBASE-LR4 compliant
- CFP2 MSA Compliance
- ITU-T G.959.1 2012
- Up to 10km for G.652 SMF
- Cooled 4x25G LAN-WDM transmitter
- 4 x 28G Electrical Serial Interface (CEI-28G-VSR)
- MDIO management interface with Digital Diagnostic
- +3.3V power supply
- Power consumption less than 6W
- Compact size: 107.5×41.5×12.4 mm
- Operating case temperature: -5 to +70 ℃
- Duple LC Receptacle
- ROHs-6 compliant

Description

Longline's CFP2-100G-LR4 transceivers are designed for use in 100 Gigabit Ethernet links over 10km single module fiber, and it compliant to the CFP MSA CFP2 HW Specification and IEEE 802.3ba 100GBASE-LR4. Digital diagnostics are available via MDIO as specified in the CFP MSA Management Interface Specification.

The transceiver's designs are optimized for high performance and cost efficiency to provide customers the best solutions for Datacom and Telecom applications.

The transceiver is RoHS-6 compliant and lead-free per Directive 2002/95/EC.

Product Specifications

I. Absolute Maximum Ratings

The limit of the maximum value is shown as below Table 1. (If operating out the limit of the maximum value will cause permanent damage).

Parameter	Symbol	Conditions	Min.	Max	Unit	Ref.
Storage temperature(case)	Tstg		-40	+85	℃	
Relative humidity	RH	0		85	%	
Damage Threshold for Receiver	Pmax			+10.0	dBm	
Power Supply	Vcc3.3V		-0.3	+3.6	V	
	Vcc5.0V				V	
Input 3.3V LVCMOS signal level	Vi		-0.3	Vcc+0.3	V	
Input 1.2V LVCMOS signal level	Vi		-0.3	1.6	V	
ESD Sensitivity on module and all host pins	HBM	Human Body model R=1.5K,C=100pF		2000	V	

II. Recommended Operating Environment

The recommended working conditions are shown as below Table 2.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Ref.
Operating Case Temperature	Tc	0		+70	℃	
Supply voltage	Vcc 3.3V	+3.14	+3.3	+3.47	V	
Power dissipation	P			6	W	
Low Power dissipation	PLow			1	W	
In-rush Curent	I-inrush			200	mA/us	
Turn-off rush Curent	I-turnoff	-200			mA/us	
Link Distance	L	2M		10km	G.652 SMF	

III. Optical Characteristics

Table 3 -100Gb/s CFP2 Optical Specifications (100GBase-LR4)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
			Transmitter			
Channel data rate				25.7812		Gbps
Aggregate data rate				103.125		Gbps
Data rate variation			-100		+100	ppm
Lane Center Wavelength	λcT0		1294.53	1295.56	1296.59	nm
	λcT1		1299.02	1300.05	1301.09	nm
	λcT2		1303.54	1304.58	1305.63	nm
	λcT3		1308.09	1309.14	1310.19	nm
Total Average Launch Power	Pout				10.5	dBm
Average Launch Power per Lane	Peach		-4.3		4.5	dBm

Optical Modulation Amplitude per Lane	OMA		-1.3		4.5	dBm
Difference in Launch power between any two lances(OMA)					5.0	dB
Launch power in OMA minus TDP, per lane	Poma tdp		-2.3			dBm
Average Launch Power of TX_DIS Transmitter per lane	Poff	TX_DIS=H			-30	dBm
Extinction Ratio	ER		4			dB
SMSR	SMSR		30			dB
Dispersion Penalty	DP	10km SMF			2.2	dB
Relative Intensity Noise	RIN	Mod off			-130	dB/Hz
Opitcal Return Loss Tolerance	TRL				20	dB
Transmitter reflectance	Tef				-12	dB
Optical Eye Mask {X1, X2, X3, Y1, Y2, Y3}1	EM		{0.25, 0.4, 0.45, 0.25, 0.28,0.4}			
			Receiver			
Channel data rate				25.7812		Gbps
Data rate variation			-100		+100	ppm
Lane Center Wavelength	λcT0		1294.53	1295.56	1296.59	nm
	λcT1		1299.02	1300.05	1301.09	nm
	λcT2		1303.54	1304.58	1305.63	nm
	λcT3		1308.09	1309.14	1310.19	nm
Damage threshold	PDT			5.5		dBm
Average receiver power per lane	Rpow		-10.6		4.5	dBm
Receive power OMA per Lane	Rovl				4.5	dBm
Difference in receive power between any two lanes(OMA)					5.5	dB
Receiver Sensitivity(OMA) per lane	Psen				-8.6	dBm

Stressed Receiver Sensitivity per Lane	Psen_str				-6.8	dBm
Receiver Reflectance	Ref				-26	dB
Conditions of stressed receiver sensitivity test						
Vertical eye closure penalty per Lane					1.8	dB
Stressed eye jitter per Lane					0.3	UI
Rx-Lane LOS Assert			-25			dBm
Rx-Lane LOS De-assert					-13	dBm
Rx-Lane LOS Hysteresis			0.5			dB

Note1. Please refer to Figure 1

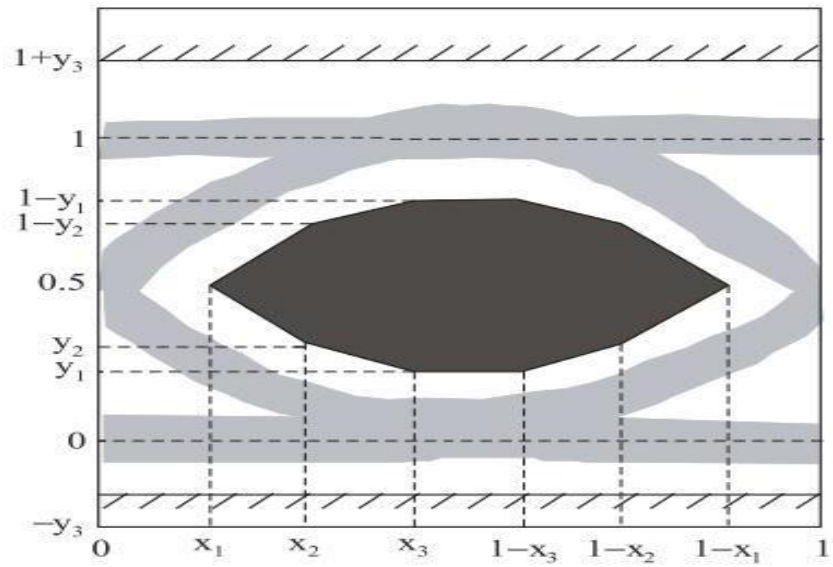


Figure 1 - Transmission eye mask definition

Table 4 -100Gb/s CFP2 Optical Specifications (OTU4)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Transmitter						
Channel data rate				27.9525		Gbps
Aggregate data rate				111.809		Gbps
Data rate variation			-20		+20	ppm
Lane Center Wavelength	λcT0		1294.53	1295.56	1296.59	nm
	λcT1		1299.02	1300.05	1301.09	nm
	λcT2		1303.54	1304.58	1305.63	nm
	λcT3		1308.09	1309.14	1310.19	nm
Total Average Launch Power	Pout				8.9	dBm
Average Launch Power per Lane	Peach		-2.5		2.9	dBm
Optical Modulation Amplitude per Lane	OMA		-1.2		4.5	dBm
Difference in Launch power between any two lances(OMA)					5.0	dB
Average Launch Power of TX_DIS Transmitter per lane	Poff	TX_DIS=H			-30	dBm
Extinction Ratio	ER		7			dB
SMSR	SMSR		30			dB
Relative Intensity Noise	RIN	Mod off			-130	dB/Hz
Opitcal Return Loss Tolerance	TRL				20	dB
Transmitter reflectance	Tef				-12	dB
Optical Eye Mask {X1, X2, X3, Y1, Y2, Y3}[1]	EM			{0.25, 0.4, 0.45, 0.25, 0.28,0.4}		

Receiver

Channel data rate				27.9525		Gbps
Data rate variation			-20		+20	ppm
Lane Center Wavelength	λcR0		1294.53	1295.56	1296.59	nm
	λcR1		1299.02	1300.05	1301.09	nm
	λcR2		1303.54	1304.58	1305.63	nm
	λcR3		1308.09	1309.14	1310.19	nm
Damage threshold	PDT			5.5		dBm
Average receiver power per lane	Rpow				4.5	dBm
Receiver power OMA per lane	Rovl				4.5	dBm
Difference in receive power between any two lanes(OMA)					5.5	dB
Optical path penalty					1.5	dB
Receiver Sensitivity per lane[2]	Psen				-10.3	dBm
Receiver Sensitivity(OMA) per lane[2]	Psen_OMA				-9.1	dBm
Receiver Reflectance	Ref				-26	dB
Rx-Lane LOS Assert			-25			dBm
Rx-Lane LOS Deassert					-13	dBm
Rx-Lane LOS Hysteresis			0.5			dB

Note1. Please refer to Figure 1
Note2. OTU-4 Rate, BER < 10-12 with FEC, ER > 7dB

IV. Electrical Characteristics

Table 5 - 100Gb/s CFP2 Electrical High Speed I/O Interface Specifications

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Transmitter (CAUI input interface)						
Signal Rate Per Lane				25.78125		Gb/s
Signal Rate Tolerance			-100		100	ppm
AC Common Mode inputVoltage Tolerance(RMS)					20	mV
Differential input returnloss	RI_{diff}	IEEE 802.3ba-2010	See Equation (83B–7)			dB
Total Input Jitter Tolerance	T_{jin}				0.62	UI
Deterministic Input Tolerance -Jitter	T_{din}				0.42	UI
Transmitter Input Mask (X1, X2)-Eye			(0.31, 0.5)			UI[1]
Transmitter Input Mask (Y1, Y2)-Eye			(42.5, 425)			mV[1]
Receiver (CAUI output interface)						
Signal Rate Per Lane				25.78125		Gb/s
Signal Rate Tolerance			-100		100	ppm
Single-ended output voltage	Vosig		-0.4		4	V
Output AC common-modevoltage(RMS)	VocomAC				15	mV
Output transition time	Tr	20%~80%	24			ps
Differential output returnloss		IEEE802.3ba-2010	See Equation (83B–5)			dB
Total Jitter	Tj				0.4	UI
Deterministic Jitter	Tdj				0.25	UI

Receiver Output Eye Mask(X1, X2)				(0.2,0.5)	UI[2]
Receiver Output Eye Mask(Y1, Y2)				(136,380)	mV[2]

Note1. refer to figure 2
Note2. refer to figure 3

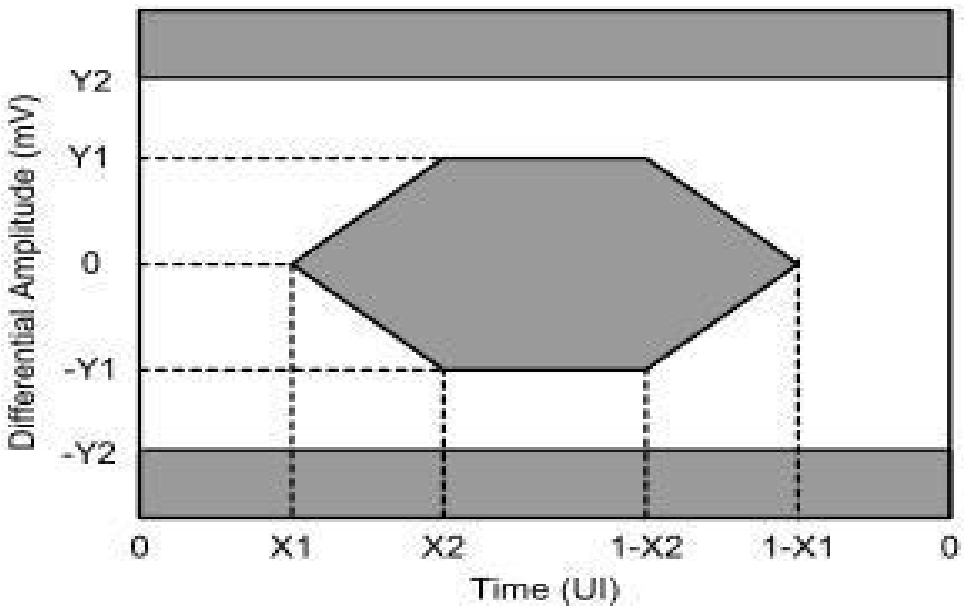


Figure 3 - CAUI transmitter eye mask

Low Speed I/O interface

Table 6 -100Gb/s CFP2 3.3V LVCMOS Electrical Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage	Vcc		3.2	3.3	3.4	V
Input High Voltage	V_{IH}		2		Vcc+0.3	V
Input Low Voltage	V_{IL}		-0.3		0.8	V
Input Leakage Current	I_{IN}		-10		+10	mA
Output High Voltage (IOH =-100uA)	V_{OH}		Vcc-0.2		Vcc+0.3	V

Output Low Voltage (IOL =100uA)	V_{OL}		-0.3		0.2	V
Minimum Pulse Width of Control Pin Signal	t_CNTL		100			us

Note:(MOD_RSTn,MOD_LOPWR,TX_DIS,PRG_CNTL,MOD_ABS,RX_LOS,GLB_ALRMn, PRG_ALRM) are LVCMOS I/O interfaces.

Table 7 - 100Gb/s CFP 1.2V LVCMOS Electrical Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input High Voltage	VI_H		0.84		1.5	V
Input Low Voltage	V_{IL}		-0.3		0.36	V
Input Leakage Current	I_{IN}		-100		+100	uA
Output High Voltage	V_{OH}		1.0		1.5	V
Output Low Voltage	V_{OL}		-0.3		0.2	V
Output High Current	I_{OH}				-4	mA
Output Low Current	I_{OL}		+4			mA
Input capacitance	C_i				10	pF

Note:(MDIO, MDC, PRTADR4:0) are 1.2V LVCMOS I/O interfaces

Table 8 - 100Gb/s CFP Timing Parameters for CFP2 Hardware Signal Pins

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
HardwareMOD_LOPWR assert	t_MOD_LOPWR_assert				1	ms
Hardware MOD_LOPWR De-assert	t_MOD_LOPWR_deassert				10	s
Receiver Loss of Signal Assert Time	t_loss_assert				100	us

Receiver Loss of Signal De-Assert Time	t_loss_deassert				100	us
Global Alarm Assert Delay Time	GLB_ALRMn_assert				150	ms
Global Alarm De-AssertDelay Time	GLB_ALRMn_deassert				150	ms
Management Interface ClockPeriod	t_prd		250			ns
Host MDIO t_setup	t_setup		10			ns
Host MDIO t_hold	t_hold		10			ns
CFP MDIO t_delay	t_delay		0		175	ns
Initialization time from Reset	t_initialize				2.5	s
Transmitter Disabled(TX_DIS asserted)	t_de-assert				100	us
Transmitter Enabled(TX_DIS de-asserted)	t_assert				2	ms

Table 9 - 100Gb/s CFP MDIO and MDC Timing Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Management Interface Clock Frequency	F_MDC		0.1		4	MHz
Management Interface Clock Period	t_prd		250		10000	ns
Host MDIO t_setup	t_setup		10			ns
Host MDIO t_hold	t_hold		10			ns
CFP MDIO t_delay1	t_delay		0		175	ns
MDC high and low time	twidth		40		60	%
			160			ns
MDIO/MDC termination in CFP	Zt		100			kOhm

Note1. Delay from MDC rising edge to MDIO data change

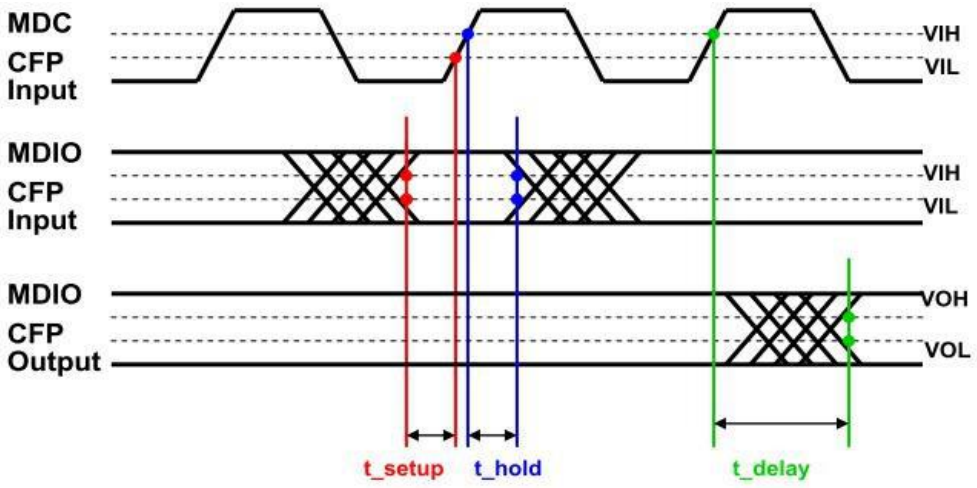


Figure 4 -100Gb/s CFP MDIO & MDC Timing Diagram

Clock interface

Table 10 - 100Gb/s CFP Reference Clock Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Impedance	Zd		80	100	120	ohm
Frequency			1/64 of host lane rate			
Frequency Stability	Xf		-100		+100	ppm[1]
			-20		+20	ppm[2]
Input Differential Voltage	Vdiff		400		1200	mV[3]
RMS Jitter	σ				10	ps[4]
Clock Duty Cycle			40		60	%
Clock Rise/Fall Time 10/90%	Tr/f		200		1250	ps[5]

Note1. For Ethernet applications **Note2.** For Telecom applications
Note3. Peak to Peak Differential
Note4. Random Jitter. Over frequency band of 10kHz < f < 10MHz
Note5. 1/64 of electrical lane

Table 11 - 100Gb/s CFP Transmitter & Receiver Monitor Clock Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Impedance	Zd		80	100	120	ohm
Frequency			1/8 of network lane rate			
Ouput Differential Voltage	Vdiff		400		1200	mV[1]
Clock Duty Cycle			40		60	%

Note1. Peak to Peak Differential

V. 100Gb/s CFP Function Diagram

Internal reference structure

The internal structure of 100Gb/s CFP shown as Figure 5.

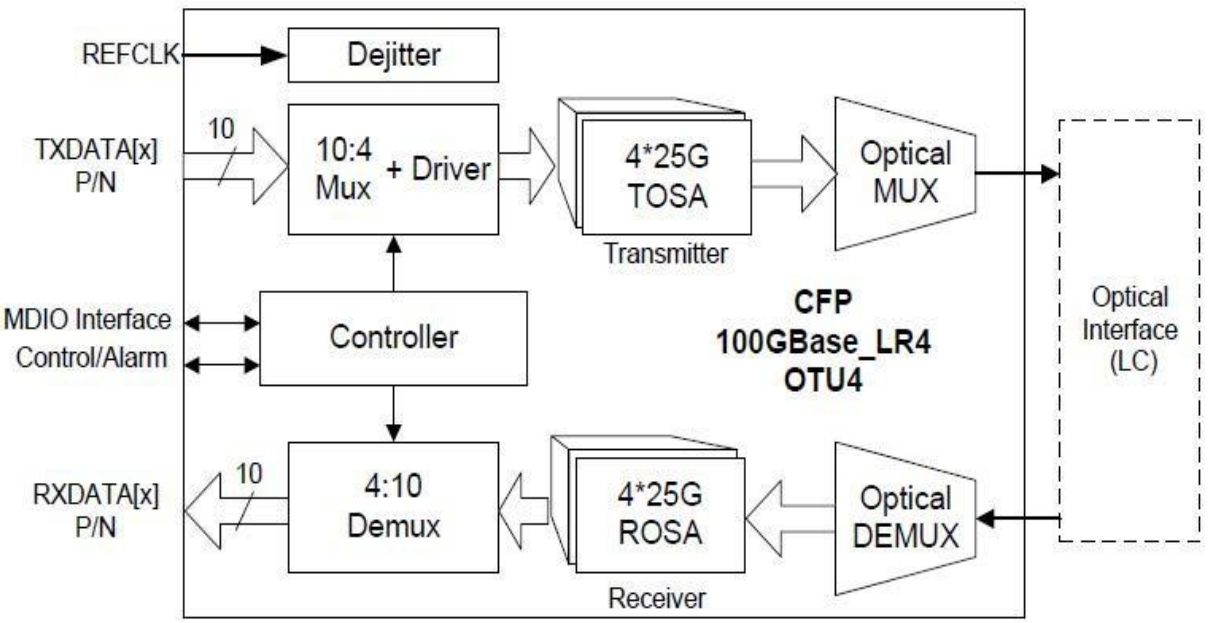


Figure 5 -10km 100Gb/s CFP2 internal structure

VI.Recommended Interface Circuit

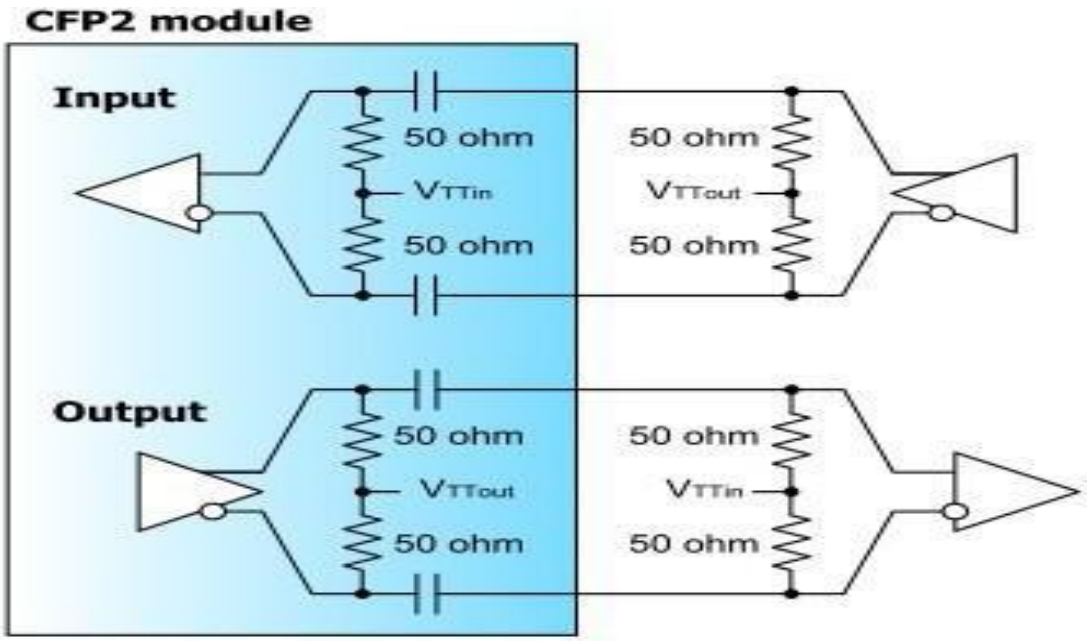


Figure 6 - Recommended High Speed I/O for Data and Clocks

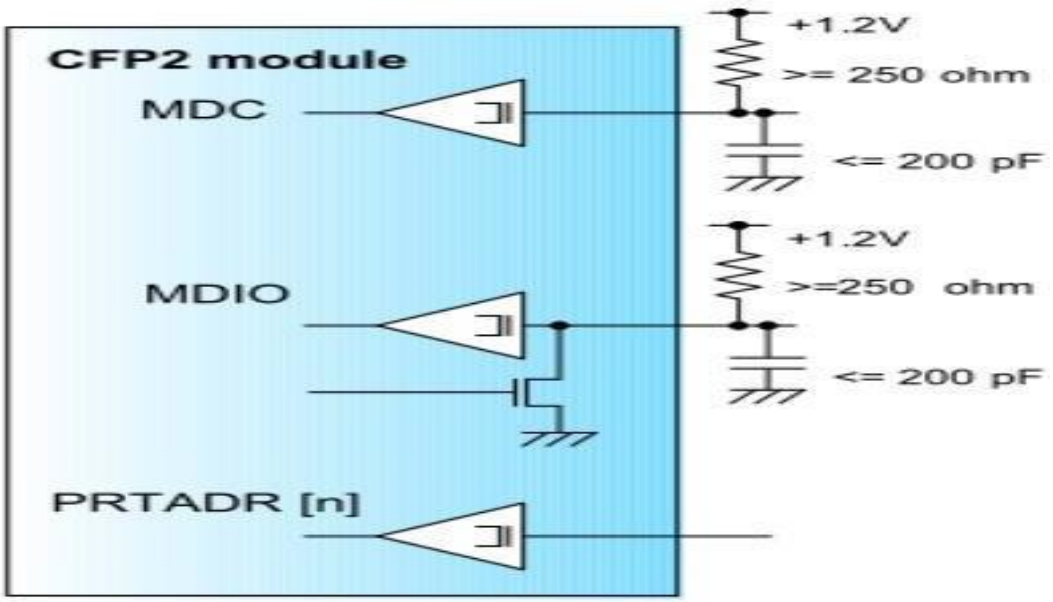


Figure 7 - Recommended MDIO Interface Termination

VII.Pin Layout

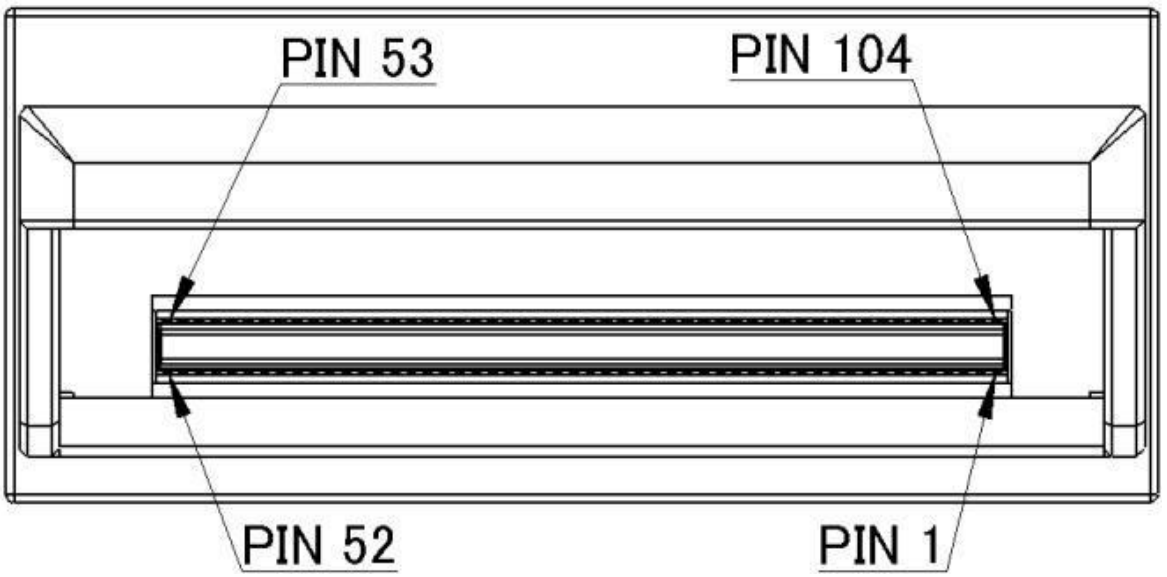
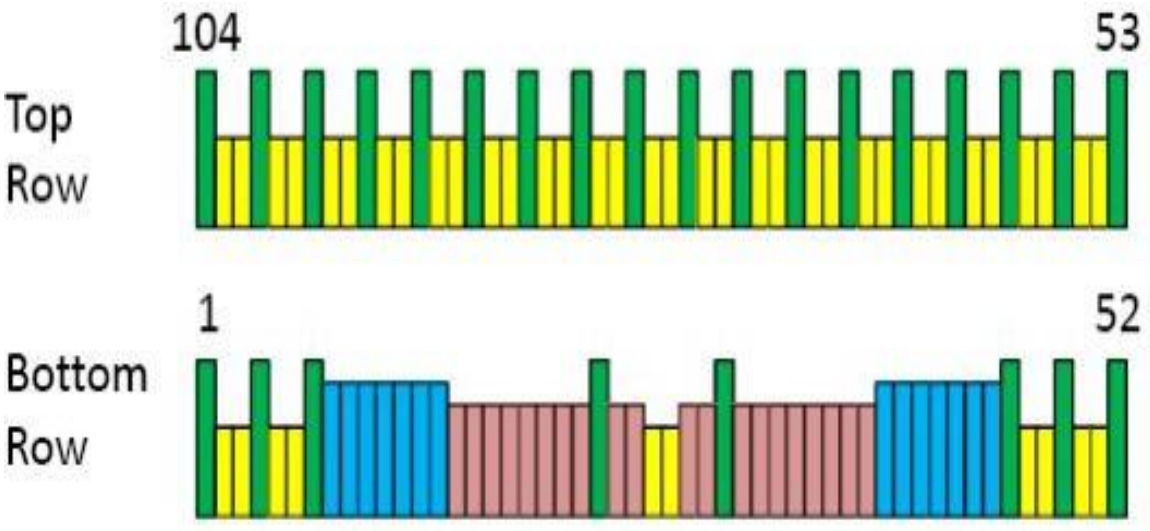


Figure 8 - CFP2 Module Pad Layout



IX. 100Gb/s CFP Mechanical Specifications

100Gb/s CFP2 mechanical dimensions should be compliant with CFP2 MSA specification.

Detailed dimensions are shown in Figure 10.

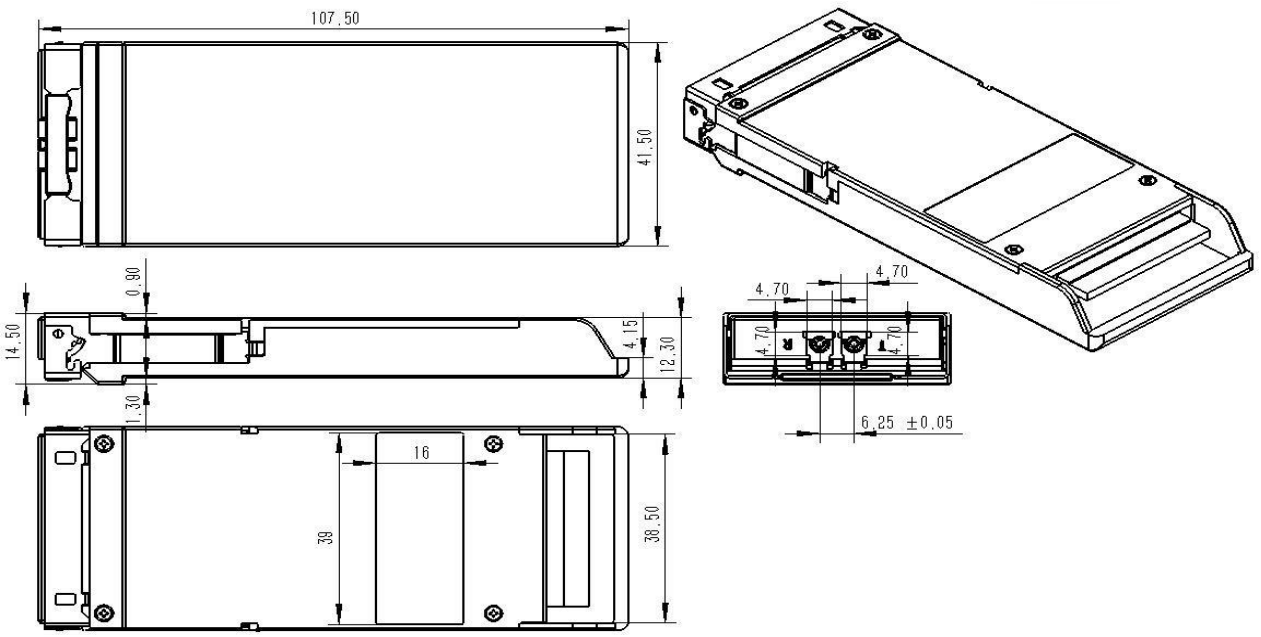


Figure 10 - 100Gb/s CFP2 Mechanical Dimensions(unit:mm)

X. Management Interface

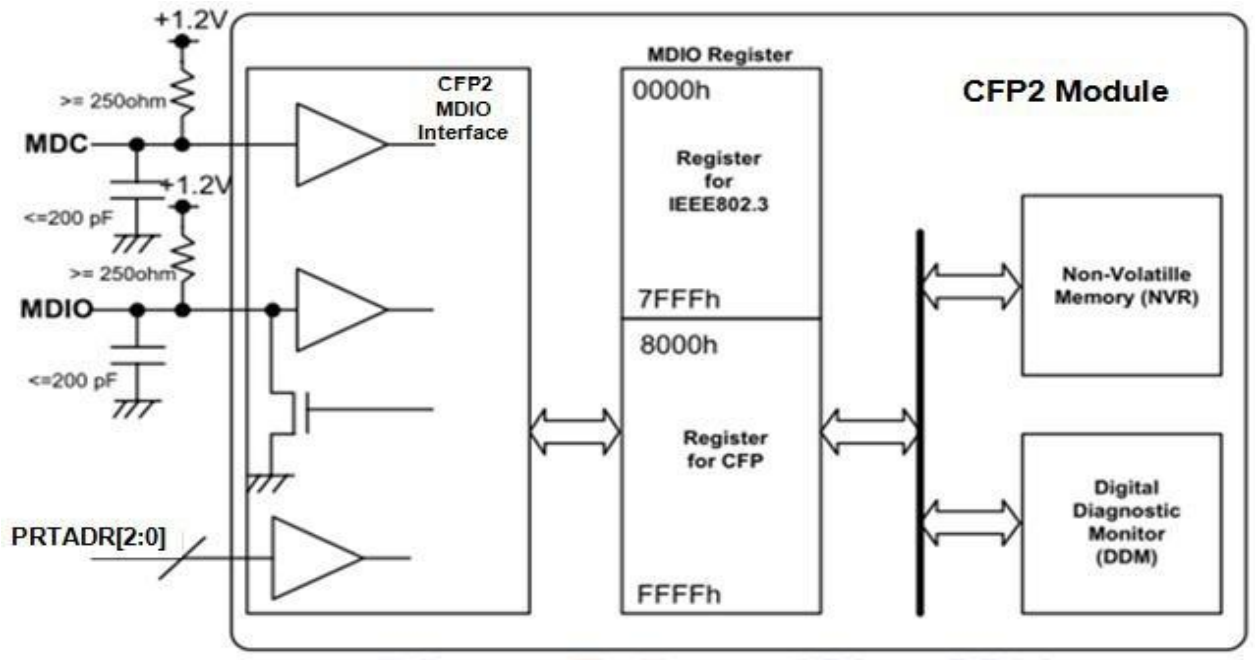


Figure 12 - CFP MDIO Interface