10GBASE-SR XFP 850nm 300m DOM Transceiver

AXM751-LL

Application

- 10GBASE-SR/SW Ethernet
- 1200-Mx-SN-I 10G Fibre Channel
- SONET OC-192/SDH STM-64
- Other optical links

Features

- Support multi protocol from 9.95Gb/s to 11.3Gb/s
- Hot pluggable 30 pin connector
- Compliant with XFP MSA
- Transmission distance of 300m over multi mode fiber
- 850nm Vcsel laser transmitter.
- Duplex LC connector
- 2-wire interface for management and diagnostic monitor
- XFI electrical interface with AC coupling
- Single power supply voltages : +3.3V
- Temperature range 0°C to 70°C
- Power dissipation: < 1.5W
- RoHS Compliant Part

Description

Longline' AXM751-LLSmall Form Factor 10Gb/s (XFP) transceivers are compliant with the current XFP Multi-Source Agreement (MSA) Specification . The high performance uncooled 850 nm Vcsel transmitter and high sensitivity PIN receiver provide superior performance

for 10G Fibre Channel and Ethernet applications up to 300m optical links.

Product Specifications

I. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Storage Temperature	T_{ST}	-40	+85	℃
Case Operating Temperature	T_{oP}	0	+70	℃
Supply Voltage	V_{CC}	-0.5	+4.0	V

II. Electrical Characteristics (Condition: T_a=T_{OP})

Parameter	Symbol	Min	Typ.	Max	Unit	Ref.
Supply Voltage	Vcc	3.13		3.45	V	
Supply Current	Icc			380	mA	
Module total power	P			1.5	W	
Transmitter						
Input differential impedance	Rin		100		Ω	1
Differential data input swing	Vin,pp	150		820	mV	
Transmit Disable Voltage	V_D	2.0		Vcc	V	
Transmit Enable Voltage	V_{EN}	GND		GND+ 0.8	V	
Transmit Disable Assert Time	T_off			100	ms	
Tx Enable Assert Time	T_on			100	ms	

Receiver						
Differential data output swing	Vout,pp	300	500	850	mV	
Data output rise time	tr			35	ps	2
Data output fall time	tf			35	ps	2
LOS Fault	$V_{LOS\ fault}$	Vcc – 0.5		VccHOST	V	3
LOS Normal	$V_{LOS\ norm}$	GND		GND+0.5	V	3
Power Supply Rejection	PSR	See Note 4 below				4

Note (1): After internal AC coupling.

Note (2): 20 – 80 %.

Note (3): Loss Of Signal is open collector to be pulled up with a 4.7k – 10kohm resistor to 3.15 – 3.6V. Logic 0 indicates normal operation; logic 1 indicates no signal detected.

Note (4): Per Section 2.7.1. in the XFP MSA Specification.

III. Optical Characteristics (Condition: Ta=T_{OP})

Parameter	Symbol	Min	Typ.	Max	Unit	Ref.
Transmitter						
Operating Date Rate	BR	9.95		11.3	Gb/s	
Bit Error Rate	BER			10-12		
Launch Power	P_{out}	-6		-1	dBm	1
Optical Wavelength	λ	840	850	860	nm	
Optical Extinction Ratio	ER	3.5			dB	
RMS Spectral Width	$λ_{RMS}$			0.45	nm	
Sidemode Supression ratio	SSRmin	30			dB	

Rise/Fall Time (20%~80%)	Tr/Tf			35	ps	
Average Launch power of OFF Transmitter	P_{OFF}			-30	dBm	
Tx Jitter	Txj	Compliant with each standard requirements				
Optical Eye Mask		IEEE802.3ae				2
Receiver						
Operating Date Rate	BR	9.95		11.3	Gb/s	
Receiver Sensitivity	Sen			-11.1	dBm	2
Maximum Input Power	P_{MAX}	0			dBm	2
Optical Center Wavelength	λ_C	780		860	nm	
Receiver Reflectance	Rrx			-12	dB	
LOS De-Assert	LOS_D			-12	dBm	
LOS Assert	LOS_A	-30			dBm	
LOS Hysteresis	LOS_H	0.5		5	dB	

Note (1): The optical power is launched into MMF.

Note (2): Measured with a PRBS 2^{31}-1 test pattern @10.3125Gbps BER<10^{-12}.

IV. Pin Assignment

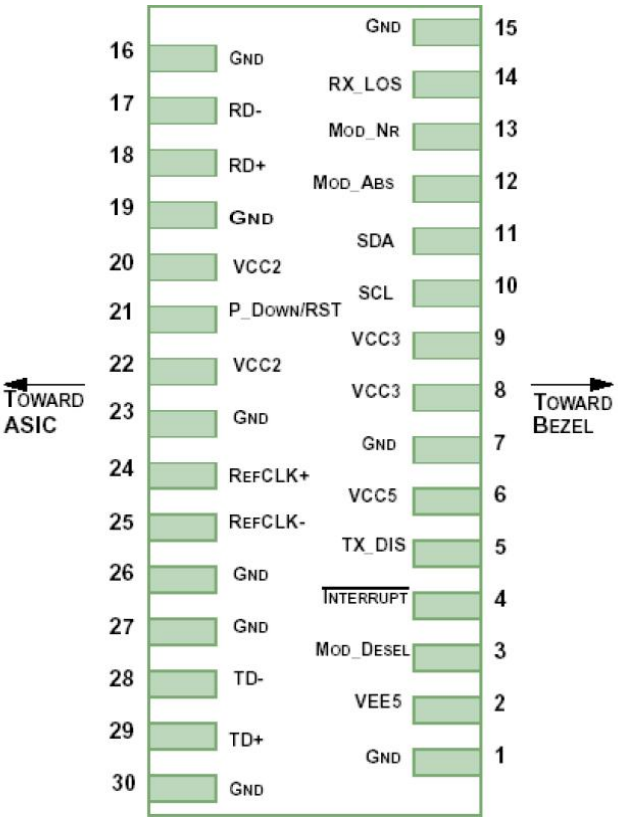


Diagram of Host Board Connector Block Pin Numbers and Name

V. Pin Description

Pin NO.	Logic	Symbol	Name/Description	Ref.
1		GND	Module Ground	1
2		VEE5	Optional –5.2 Power Supply – Not required	
3	LVTTL-I	Mod-Desel	Module De-select; When held low allows the module to ，respond to 2-wire serial interface commands	
4	LVTTL-O	Interrupt	Interrupt (bar); Indicates presence of an important condition which can be read over the serial 2-wire interface	2
5	LVTTL-I	TX_DIS	Transmitter Disable; Transmitter laser source turned off	
6		VCC5	+5 Power Supply	
7		GND	Module Ground	1

8		VCC3	+3.3V Power Supply	
9		VCC3	+3.3V Power Supply	
10	LVTTL-I	SCL	Serial 2-wire interface clock	2
11	LVTTL- I/O	SDA	Serial 2-wire interface data line	2
12	LVTTL-O	Mod_Abs	Module Absent; Indicates module is not present. Grounded in the module.	2
13	LVTTL-O	Mod_NR	Module Not Ready;	2
14	LVTTL-O	RX_LOS	Receiver Loss of Signal indicator	2
15		GND	Module Ground	1
16		GND	Module Ground	1
17	CML-O	RD-	Receiver inverted data output	
18	CML-O	RD+	Receiver non-inverted data output	
19		GND	Module Ground	1
20		VCC2	+1.8V Power Supply – Not required	
21	LVTTL-I	P_Down/RST	Power Down; When high, places the module in the low power stand-by mode and on the falling edge of P_Down initiates a module reset Reset; The falling edge initiates a complete reset of the module including the 2-wire serial interface, equivalent to a power cycle.	1
22		VCC2	+1.8V Power Supply – Not required	
23		GND	Module Ground	1
24	PECL-I	RefCLK+	Reference Clock non-inverted input, AC coupled on the host board – Not required	3
25	PECL-I	RefCLK-	Reference Clock inverted input, AC coupled on the host board – Not required	3
26		GND	Module Ground	1
27		GND	Module Ground	1
28	CML-I	TD-	Transmitter inverted data input	
29	CML-I	TD+	Transmitter non-inverted data input	
30		GND	Module Ground	1

Note (1): Module circuit ground is isolated from module chassis ground within the module.

Note (2): Open collector; should be pulled up with 4.7k – 10k ohms on host board to a voltage between 3.15V and 3.6V.

Note (3): A Reference Clock input is not required .

VI. Digital Diagnostic Functions

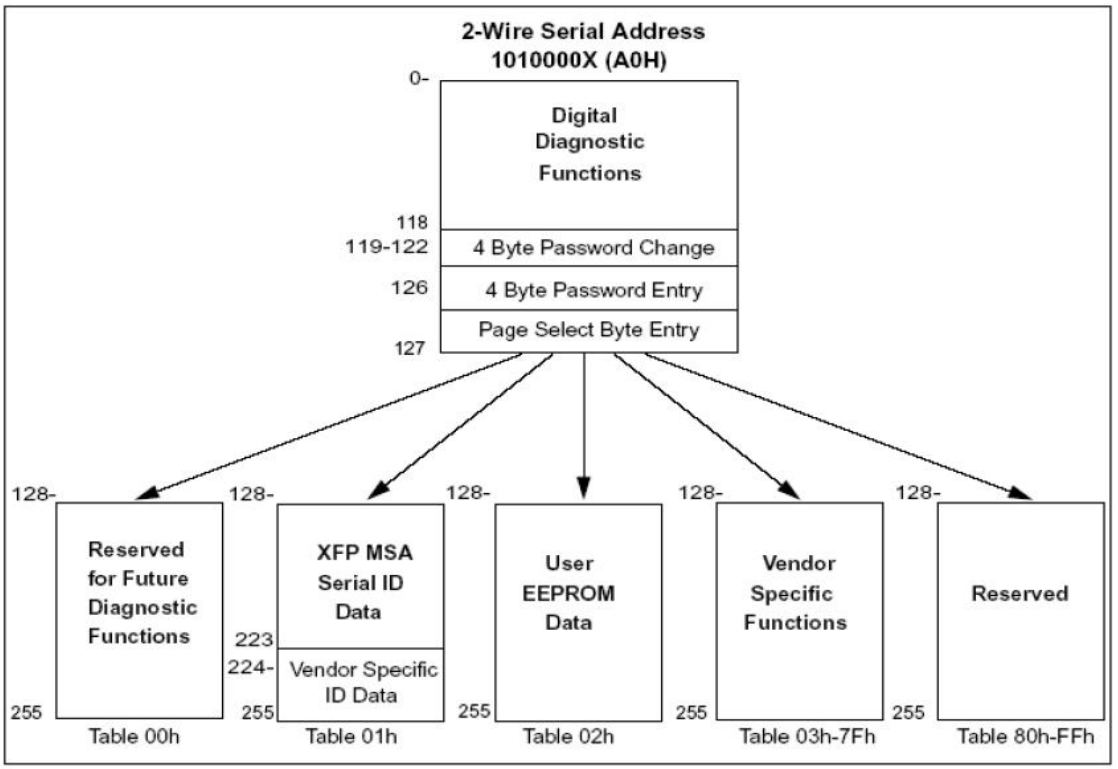
As defined by the XFP MSA 1 , Longline's XFP transceivers provide digital diagnostic functions via a 2-wire serial interface, which allows real-time access to the following operating parameters:

- ✓ Transceiver temperature
- ✓ Laser bias current
- ✓ Transmitted optical power
- ✓ Received optical power
- ✓ Transceiver supply voltage

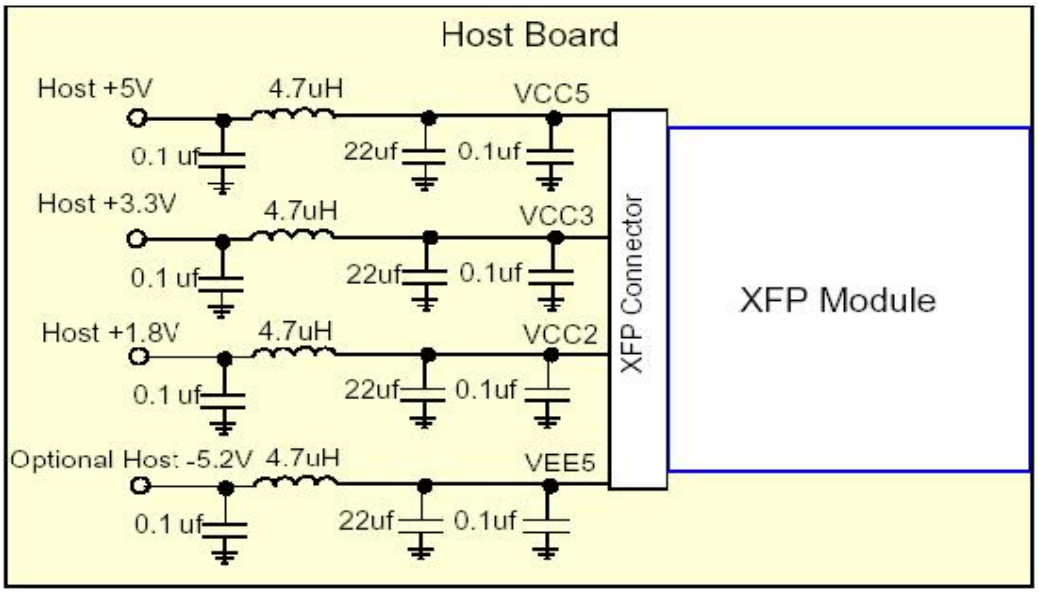
It also provides a sophisticated system of alarm and warning flags, which may be used to alert end-users when particular operating parameters are outside of a factory-set normal range.

The operating and diagnostics information is monitored and reported by a Digital Diagnostics Transceiver Controller (DDTC) inside the transceiver, which is accessed through the 2-wire serial interface. When the serial protocol is activated, the serial clock signal (SCL pin) is generated by the host. The positive edge clocks data into the XFP transceiver into those segments of its memory map that are not write-protected. The negative edge clocks data from the XFP transceiver. The serial data signal (SDA pin) is bi-directional for serial data transfer. The host uses SDA in conjunction with SCL to mark the start and end of serial protocol activation. The memories are organized as a series of 8-bit data words that can be addressed individually or sequentially. The 2-wire serial interface provides sequential or random access to the 8 bit parameters, addressed from 000h to the maximum address of the memory.

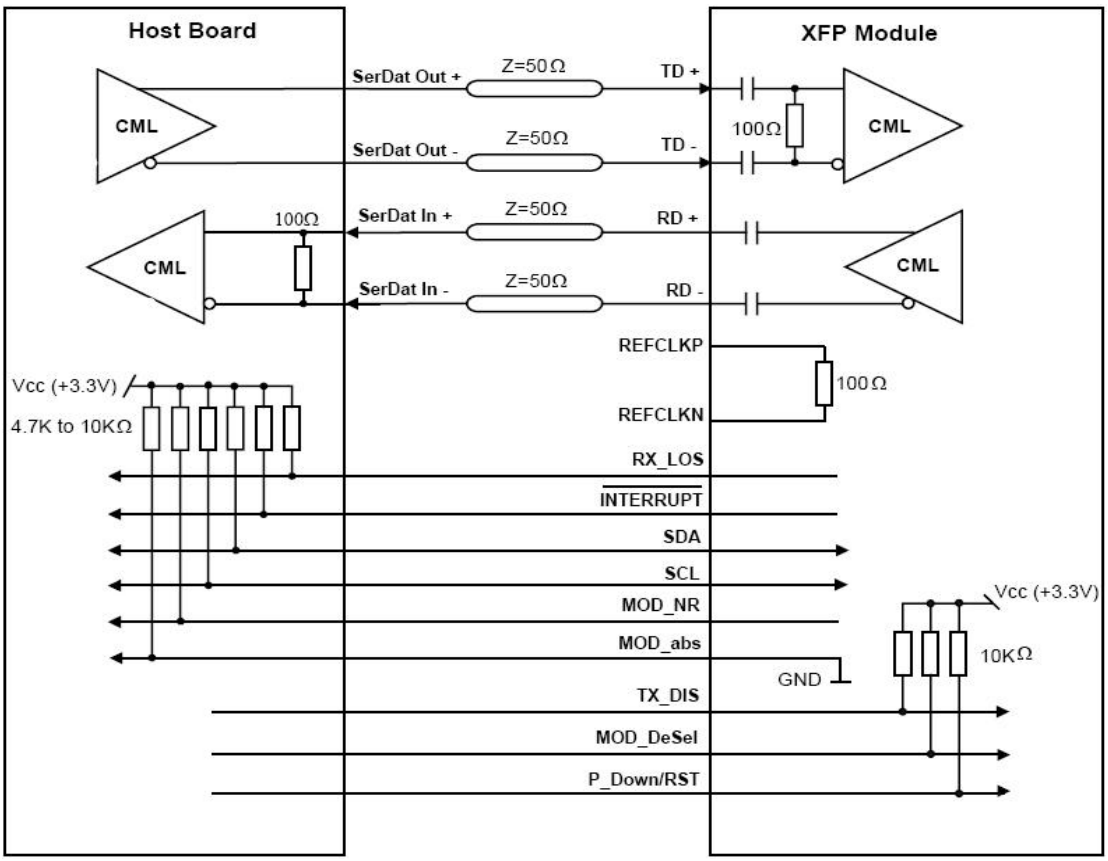
For more detailed information including memory map definitions, please see the XFP MSA Specification.



VII. Recommended Circuit

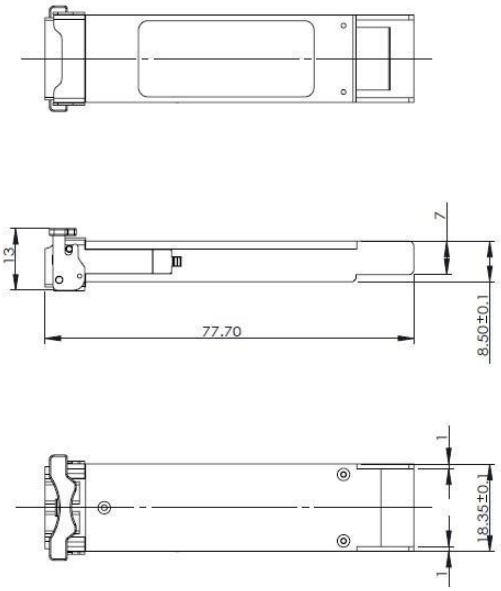


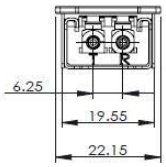
Recommended Host Board Power Supply Circuit

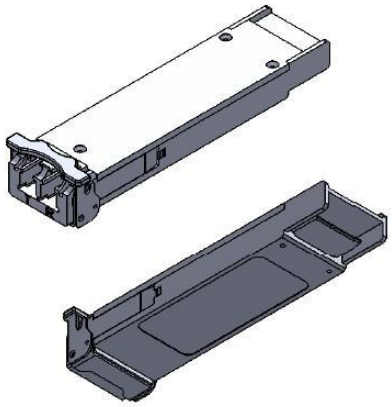


Recommended High-speed Interface Circuit

VIII. Mechanical Dimensions







XI.Mechanical Dimensions