40GBASE-LR4L QSFP+ 1310nm 2km LC Transceiver for SMF

40G-QSFP-LR4L-LL

Application

- 40GBASE-LR4L 40G Ethernet

Features

- Hot Pluggable QSFP+ form factor
- Supports 41.2 Gb/s aggregate bit rates
- Power dissipation <3.5W
- Single 3.3V power supply
- Maximum link length of 2km on Single Mode Fiber (SMF)
- Uncooled 4x10Gb/s CWDM transmitter
- XLPPI electrical interface
- Duplex LC receptacles
- Commercial operating case temperature range: 0° C to 70° C
- RoHS-6 Compliant
- Built-in digital diagnostic functions, including optical power monitoring

Description

QSFP+ transceiver modules are designed for use in 40 Gigabit per second links over single mode fiber. They are compliant with the QSFP+ MSA and IEEE 802.3ba 40GBASE-LR4. Digital diagnostics functions are available via an I2C interface, as specified by the QSFP+ MSA. The optical transceiver is compliant per the RoHS Directive 2011/65/EU.

Product Specifications

I. General Specifications

Parameter	Value	Unit	Notes
Module Form Factor	QSFP+		
Number of Lanes	4 Tx and 4 Rx		
Maximum Aggregate Data Rate	41.2	Gb/s	
Maximum Data Rate per Lane	10.3	Gb/s	Higher bit rates may be supported. Please contact Longline.
Protocols Supported	Typical applications include 40G Ethernet, Infiniband Fibre Channel, SATA/SAS3		
Electrical Interface and Pin-out	38-pin edge connector		Pin-out as defined by the QSFP+ MSA
Maximum Power Consumption	3.5	Watts	
Management Interface	Serial, I2C-based, 400 kHz maximum frequency		As defined by the QSFP+ MSA

Data Rate Specifications	Symbol	Min	Typ.	Max	Units	Ref.
Bit Rate per Lane	BR			10313	Mb/sec	1
Bit Error Ratio	BER			10^{-12}		2
Link distance on SMF-28	d			2	kilometers	3

Notes:

1. Compliant with 40GBASE-LR4 and XLPPI per IEE 802.3ba. Compatible with 1/10 Gigabit Ethernet and 1/2/4/8/10G Fibre Channel.
2. Tested with a PRBS 2^{31}-1 test pattern.
3. Per 40GBASE-LR4, IEEE 802.3ba.

II. Absolute Maximum Ratings

Parameter	Symbol	Min	Typ.	Max	Unit	Ref.
Maximum Supply Voltage	Vcc1, VccTx, VccRx	-0.5		3.6	V	
Storage Temperature	Ts	-40		85	° C	
Case Operating Temperature	Top	15		60	° C	
Relative Humidity	RH	0		85	%	1
Damage Threshold, per Lane	DT	3.4			dBm	

Note:
1.Non-condensing.

III. Electrical Characteristics

Parameter	Symbol	Min	Typ.	Max	Unit	Ref.
Supply Voltage	Vcc1, VccTx, VccRx	3.1		3.47	V	
Supply Current	Icc			1.13	A	
Transmit turn-on time				2000	ms	1
	Transmitter (per Lane)					
Single ended input voltage tolerance	VinT	-0.3		4.0	V	
Differential data input swing	Vin,pp	120		1200	mVpp	2
Differential input threshold			50		mV	
AC common mode input voltage tolerance (RMS)		15			mV	
Differential input return loss		Per IEEE P802.3ba,Section 86A.4.1.1			dB	3

J2 Jitter Tolerancez	Jt2	0.17			UI	
J9 Jitter Tolerance	Jt9	0.29			UI	
Data Dependent Pulse Width Shrinkage	DDPWS	0.07			UI	
Eye mask colordinates {X1, X2 ,Y1, Y2}			0.11, 0.31 95, 350		UI mV	4
Receiver (per Lane)						
Single-ended output voltage		-0.3		4.0	V	
Differential data output swing	Vout,pp	200		400	mVpp	5,6
		300		600		
		400	550	800		
		600		1200		
AC common mode output voltage (RMS)				7.5	mV	
Termination mismatch at 1 MHx				5	%	
Differential output return loss		Per IEEE P802.3ba,Section 86A.4.2.1			dB	3
Common mode output return loss		Per IEEE P802.3ba,Section 86A.4.2.2			dB	3
Output transition time, 20% to 80%		28			ps	
J2 Jitter output	Jo2			0.42	UI	
J9 Jitter output	Jo9			0.65	UI	
Eye mask coordinates #1 {X1, X2, Y1, Y2}			0.29, 0.5 150, 425		UI mV	4
Power Supply Ripple Tolerance	PSR	50			mVpp	

Notes:

1. From power-on and end of any fault conditions.
2. After internal AC coupling. Self-biasing 100Ωdifferential input.
3. 10 MHz to 11.1 GHz range
4. Hit ratio = 5 x 10E-5.
5. AC coupled with 100Ωdifferential output impedance.
6. Output voltage is settable in 4 discrete steps via the I2C. Default is 400-800 mV.

IV. Optical Characteristics (TOP = 0 to 70℃, VCC = 3.1 to 3.47 Volts)

Parameter	Symbol	Min	Typ.	Max	Unit	Ref.
Transmitter (per Lane)						
Signaling Speed per Lane				10.3125	GBd	1
Lane Center wavelengths (range)			1264.5-1277.5 1284.5-1297.5 1304.5-1317.5 1324.5-1337.5		nm	
Total Average Launch Power	Pout			8.3	dBm	
Average Launch Power per Lane	TXPx	-7.0		2.3	dBm	
Transmit OMA per Lane	TxOMA	-4.0		3.5	dBm	2
Optical Extinction Ratio	ER	3.5			dB	
Sidemode Suppression ratio	SSRmin	30			dB	
Average launch power of OFF transmitter, per lane				-30	dBm	
Relative Intensity Tolerance	RIN			-128	dB/Hz	3
Optical Return Loss Tolerance				20		
Transmitter Reflectance				-12	dB	
Transmitter eye mask definition {X1, X2, X3, Y1, Y2, Y3}		(0.25, 0.4, 0.45, 0.25, 0.28, 0.4)				

Parameter	Symbol	Min	Typ.	Max	Unit	Ref.
Receiver (per Lane)						
Signaling Speed per Lane				10.3125	GBd	4
Lane Center wavelengths (range)			1264.5-1277.5 1284.5-1297.5 1304.5-1317.5 1324.5-1337.5		nm	
Receive Power (OMA) per Lane	RxOMA			3.5	dBm	
Average Receive Power per Lane	RXP_x	-11.5		2.3	dBm	5
Receiver Sensitivity (OMA) per Lane	Rxsens			-11.5	dBm	

Stressed Receiver Sensitivity (OMA) per Lane	SRS			-9.6	dBm	
Damage Threshold per Lane	P_{MAX}			3.4	dBm	
Return Loss	RL			-26	dB	
Vertical eye closure penalty, per lane				1.9	dB	
Receive electrical 3dB upper cutoff frequency, per lane				12.3	GHz	
LOS De-Assert	LOS_D			-15	dBm	
LOS Assert	LOS_A	-28			dBm	
LOS Hysteresis			1		dB	

Notes:

1. Transmitter consists of 4 lasers operating at 10.3Gb/s each.
2. Minimum value is informative.
3. RIN is scaled by 10*log(10/4) to maintain SNR outside of transmitter.
4. Receiver consists of 4 photodetectors operating at 10.3Gb/s each.
5. Minimum value is informative, equals min TxOMA with infinite ER and max channel insertion loss.

V. Pin Description

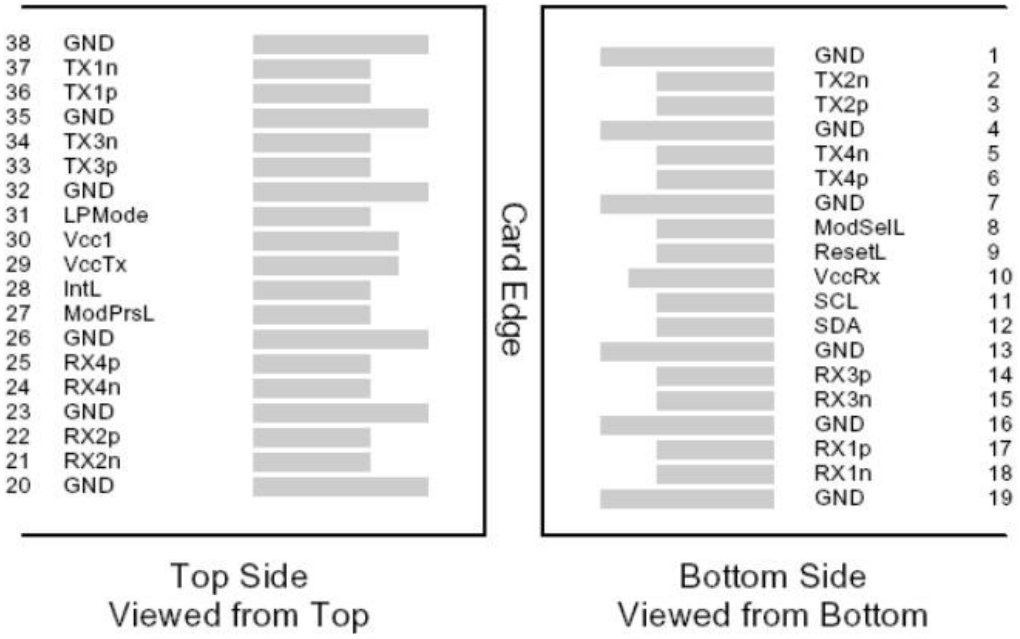

Figure 1 – QSFP+ MSA-compliant 38-pin connector

Pin	Symbol	Name/Description	Notes
1	GND	Ground	1
2	Tx2n	Transmitter Inverted Data Input	
3	Tx2p	Transmitter Non-Inverted Data Input	
4	GND	Ground	1
5	Tx4n	Transmitter Inverted Data Input	
6	Tx4p	Transmitter Non-Inverted Data Input	
7	GND	Ground	1
8	ModSelL	Module Select	
9	ResetL	Module Reset	

10	Vcc Rx	+3.3 V Power supply receiver	
11	SCL	2-wire serial interface clock	
12	SDA	2-wire serial interface data	
13	GND	Ground	1
14	Rx3p	Receiver Non-Inverted Data Output	
15	Rx3n	Receiver Inverted Data Output	
16	GND	Ground	1
17	Rx1p	Receiver Non-Inverted Data Output	
18	Rx1n	Receiver Inverted Data Output	
19	GND	Ground	1
20	GND	Ground	1
21	Rx2n	Receiver Inverted Data Output	
22	Rx2p	Receiver Non-Inverted Data Output	
23	GND	Ground	1
24	Rx4n	Receiver Inverted Data Output	
25	Rx4p	Receiver Non-Inverted Data Output	
26	GND	Ground	1
27	ModPrsL	Module Present	
28	IntL	Interrupt	
29	Vcc Tx	+3.3 V Power supply transmitter	
30	Vcc1	+3.3 V Power Supply	
31	LPMode	Low Power Mode	
32	GND	Ground	1
33	Tx3p	Transmitter Non-Inverted Data Input	33

34	Tx3n	Transmitter Inverted Data Input	
35	GND	Ground	1
36	Tx1p	Transmitter Non-Inverted Data Input	
37	Tx1n	Transmitter Inverted Data Input	
38	GND	Ground	1

Note:

Circuit ground is internally isolated from chassis ground.

VI. Mechanical Specifications

The mechanical specifications are compliant to the QSFP+ MSA transceiver module specifications.