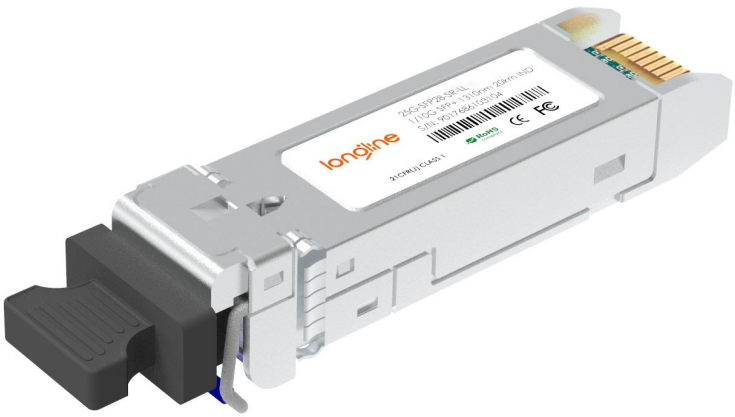
25G SFP28 850nm 100m DOM Transceiver

25G-SFP28-SR-LL



Application

- 25GBASE-SR Ethernet

Standards

- SFF-8472
- SFF-8024
- SFF-8431
- SFF-8432

Features

- Supports 25.78Gb/s Bit Rate
- Hot-pluggable SFP+ Footprint
- 850nm VCSEL Laser and PIN Photo-detector
- Internal CDR on Transmitter and Receiver Channel
- RoHS-10 Compliant
- Link Lengths at 25.78G 100m Over OM4 MMF
- LC Duplex Connector
- Low Power Consumption < 1W
- 0℃ to 70℃ Operating Temperature Range
- Single +3.3V±5% Power Supply
- Programmable TX Input Equalizer
- Programmable RX Pre-emphasis
- Digital Monitoring SFF-8472 Compliant

Description

The 25G SR short-wavelength transceiver is designed for use in 25.78Gb/s data rate over multimode fiber. The transceiver is compliant with SFF-8431, and the mechanical SFP+ plug is compatible with SFF-8432. Digital diagnostics functions are available via a 2-wire serial interface, as specified in SFF-8472.

Product Specifications

I. Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Supply Voltage	Vcc	-0.3	+4.0	V
Storage Temperature	Ts	-40	+85	℃
Operating Humidity	RH	0	+85	%

II. General Specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit
Bit Rate	BR		25.78		Gbps
Bit Error Ratio	BER			$5*10^{E-5}$	
Max. Supported Link Length	L_{MAX}			100	m

III. Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating Temperature	Tc	0		+70	℃
Power Supply Voltage	Vcc	3.14	3.3	3.46	V
Bit Rate	BR		25.78		Gbps
Max. Supported Link Length	L_{MAX}			100	m

IV. Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply Voltage	V_{CC}	3.14	3.3	3.46	V	
Supply Current	Icc			230	mA	
			Transmitter			
Input Differential Impedance	R_{IN}	80	100	120	Ω	1
Single Ended Data Input Swing	V_{IN}	90		500	mVp-p	
Transmit Disable Voltage	V_{DIS}	2		V_{CCHOST}	V	
Transmit Enable Voltage	V_{EN}	V_{EE}		V_{EE}+0.8	V	
Transmit Fault Assert Voltage	V_{FA}	2		V_{CCHOST}	V	
Transmit Fault De-Assert Voltage	V_{FDA}	V_{EE}		V_{EE}+0.8	V	
			Receiver			
Single Ended Data Output Swing	V_{OD}	200		500	mVp-p	
LOS Fault	V_{LOSFT}	2		V_{CCHOST}	V	
LOS Normal	V_{LOSNR}	V_{EE}		V_{EE}+0.8	V	

Notes:

1. Differential between TD+ / TD–.

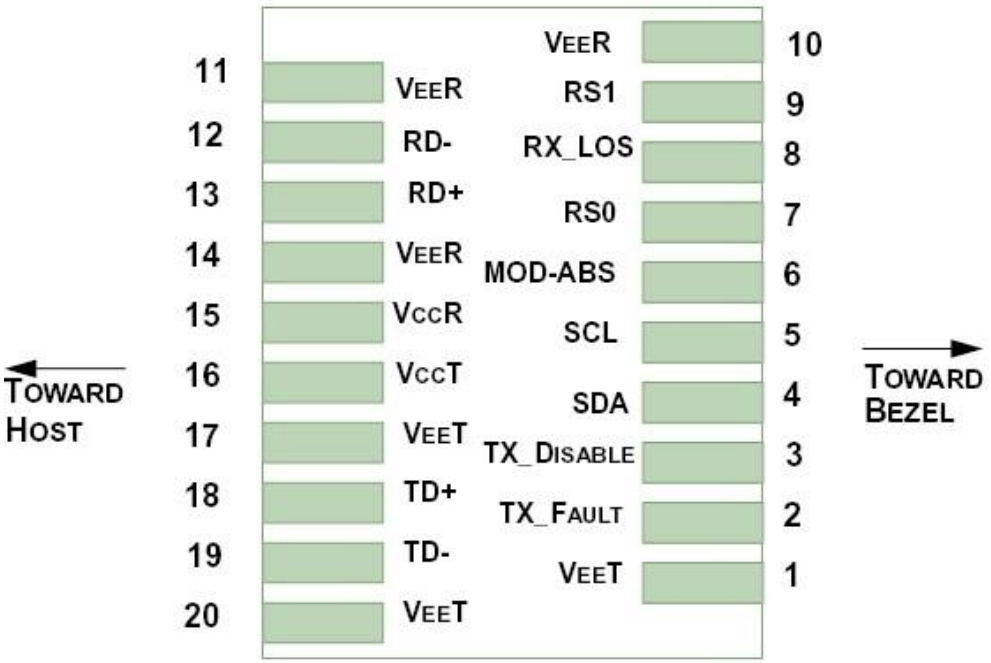
V. Optical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Transmitter						
Nominal Wavelength	λ	840		860	nm	
Spectral Width	Δλ			0.6	nm	
Optical Modulation Amplitude	POMA	-6.4		3	dBm	
Optical Output Power	Pav	-8.4		2.4	dBm	
Extinction Ratio	ER	2			dB	
Transmitter and Dispersion Penalty	TDP			5	dB	
Average Launch Power of OFF Transmitter	P_{OFF}			-30	dBm	
Receiver						
Center Wavelength	λ	840		860	nm	
Average Receiver Power	P_{AVG}	-10.3		2.4	dBm	1
Stressed Receiver Sensitivity (OMA)	R_{SENSE}			-5.2	dBm	2
Receiver Reflectance	R_{REFL}			-12	dB	
Assert LOS	LOS_A	-30			dBm	
De-Assert LOS	LOS_D			-13	dBm	
LOS Hysteresis		0.5			dB	

Notes:

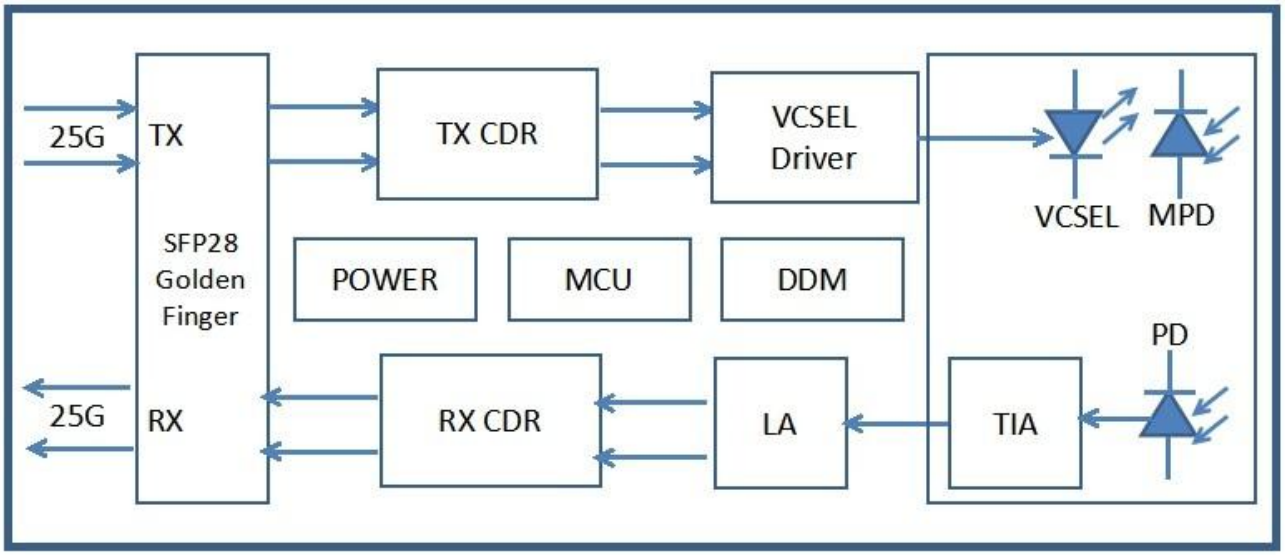
1. Sensitivity for 25.78G PRBS 231-1 and BER better than or equal to $5*10^{E-5}$.
2. The stressed sensitivity values in the table are for system level BER measurements which include the effects of CDR circuit.

VI. Pin Assignment



Pin Number	Symbol	Name	Description
1,17,20	VeeT	Transmitter Signal Ground	These pins should be connected to signal ground on the host board.
2	TX Fault	Transmitter Fault Out (OC)	Logic "1" Output = Transmitter Fault Logic "0" Output = Normal Operation This pin is open collector compatible, and should be pulled up to Host Vcc with a 10kΩ resistor.
3	TX Disable	Transmitter Disable In (LVTTL)	Logic "1" Input (or no connection) = Laser off Logic "0" Input = Laser on This pin is internally pulled up to VccT with a 10 kΩ resistor.
4	SDA	Module Definition Identifiers	Serial ID with SFF 8472 Diagnostics Module Definition pins should be pulled up to Host Vcc with 10 kΩ resistors.
5	SCL		
6	MOD-ABS		
7	RS0	Receiver Rate Select (LVTTL) Transmitter Rate Select (LVTTL)	NA
9	RS1		NA
8	LOS	Loss of Signal Out (OC)	This pin is open collector compatible, and should be pulled up to Host Vcc with a 10kΩ resistor.
10,11,14	VeeR	Receiver Signal Ground	These pins should be connected to signal ground on the host board.
12	RD-	Receiver Negative DATA Out (CML)	Light on = Logic "0" Output Receiver DATA output is internally AC coupled and series terminated with a 50Ω resistor.
13	RD+	Receiver Positive DATA Out(CML)	Light on = Logic "1" Output Receiver DATA output is internally AC coupled and series terminated with a 50Ω resistor.
15	VccR	Receiver Power Supply	This pin should be connected to a filtered +3.3V power supply on the host board. See Figure 3.Recommended power supply filter
16	VccT	Transmitter Power Supply	This pin should be connected to a filtered +3.3V power supply on the host board. See Figure 3.Recommended power supply filter
18	TD+	Transmitter Positive DATA In(CML)	Logic "1" Input = Light on Transmitter DATA inputs are internally AC coupled and terminated with a differential 100Ω resistor.
19	TD-	Transmitter Negative DATA In(CML)	Logic "0" Input = Light on Transmitter DATA inputs are internally AC coupled and terminated with a differential 100Ω resistor.

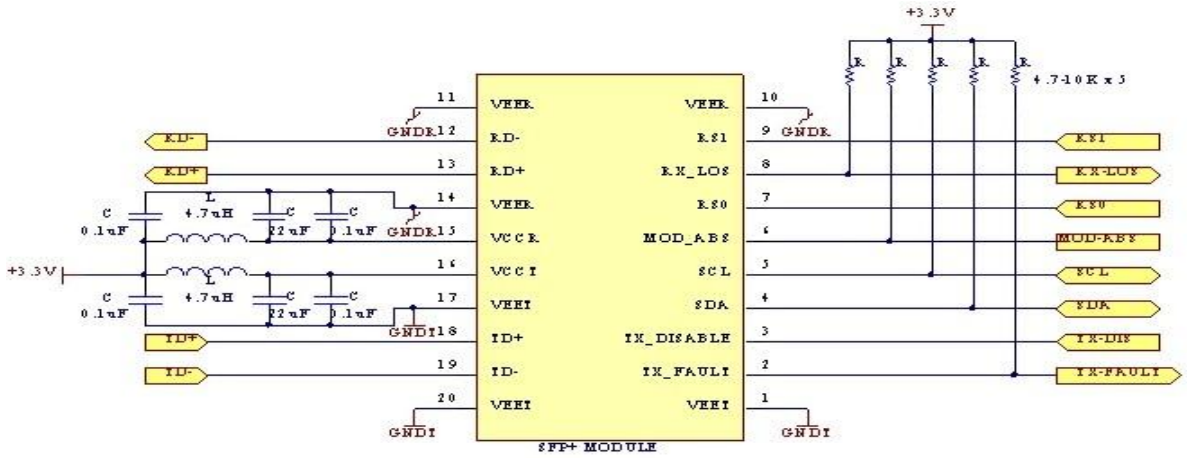
VII. Optical Module Block Diagram



VIII. Regulatory Compliance

Feature	Test Method	Performance
Electrostatic Discharge (ESD) to the Electrical Pins	MIL-STD-883C Method 3015.7	Class 1 (> 1500 Volts)
Electrostatic Discharge (ESD) Immunity	Variation of IEC 61000-4-2	LV 4(Air discharge :15KV;Contact discharge:8 KV)
Electromagnetic Interference (EMI)	CISPR22 ITE Class B EN55022 Class B FCC Class B	Compliant with standards
Immunity	IEC61000-4-3 Class 2 EN55024	Typically show no measurable effect from a 3V/m fieldswept from 80 to 1000MHz applied to the transceiver without a chassis enclosure

IX. Typical Application Circuit



X. Diagram Mechanial Drawing