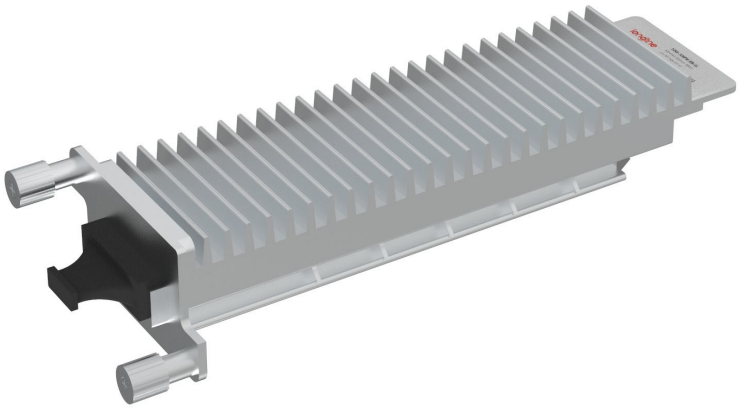
10G BIDI XFP 1270nm-TX/1330nm-RX 60km Transceiver

10G-XNPK-ER-LL



Application

- 10GBASE-ER/EW Ethernet
- SONET OC-192/SDH STM-64
- 1200-SM-LL-L 10G Fibre Channel

Standards

- IEEE 802.3ae 10GBASE-ER
- XFP MSA

Features

- Support 9.95Gb/s to 11.3Gb/s bit rates
- Hot Pluggable XFP footprint
- Single LC for Bi-directional Transmission
- Maximum link length of 60km
- Single 3.3V voltage supply
- Uncooled 1270nm CWDM DFB Laser, APD receiver
- Power dissipation < 3.5W
- No Reference Clock required
- Built-in digital diagnostic functions
- Temperature range 0° C to 70° C
- Very low EMI and excellent ESD protection
- RoHS Compliant

Description

Longline Bi-directional 10Gb/s (XFP) transceivers are compliant with the current XFP Multi-Source Agreement (MSA) Specification. They comply with 10-Gigabit Ethernet 10GBASE-ER/EW per IEEE 802.3ae, SONET OC-192 /SDH STM-64 and 10G Fibre Channel 1200-SM-LL-L. Digital diagnostics functions are available via a 2-wire serial interface, as specified in the XFP MSA.

Products Specifications

I. Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature Range	T_{ST}	-40	85	ºC
Supply Voltage	V_{CC}	-0.5	4.0	V

II. Recommended Operating Conditions

Parameter	Symbol	Min.	Typical	Max.	Unit
Operating Temperature Range	T_C	0		70	ºC
Power Supply Voltage	V_{CC}	3.13	3.3	3.45	V
Bit Rate	BR	9.95		11.3	Gb/s
Bit Error Rate	BER			10^{-12}	
Max. Supported Link Length	L			60	km

III. Optical Characteristics

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Transmitter						
Data Rate	B	9.95		11.3	Gbps	
Average Optical Power	P_{max}	1		5	dBm	1
Center Wavelength	λ	1260	1270	1280	nm	
Spectral Width	Δλ			1	nm	
Side Mode Suppression Ratio	$SMSR_{min}$	30			dB	
Average Launch Power of OFF Transmitter	P_{OFF}			-30	dBm	
Extinction Ratio	ER	6			dB	
Rise/Fall Time (20%~80%)	T_r/T_f			50	ps	
Tx Jitter	Txj	Compliant with each standard requirements				
Optical Eye Mask			IEEE802.3ae			2
Receiver						
Data Rate	BR	9.95		11.3	Gbps	
Center Wavelength	λ_C	1320	1330	1340	nm	
Receiver Sensitivity	R_{SEN}			-20	dBm	2
Maximum Input Power	P_{MAX}	-7			dBm	2
Receiver Reflectance	Rrx			-27	dB	

Parameter		Symbol	Min.	Typical	Max.	Unit	Notes
LOS	Optical Assert	LOS_A	-33			dBm	
	Optical Dessert	LOS_D			-21	dBm	
LOS Hysteresis		LOS_H	0.5		5	dB	

Notes

1. The optical power is launched into SMF.
2. Measured with a PRBS 2^{31}-1 test pattern @10.3125Gbps BER<10^{-12}.

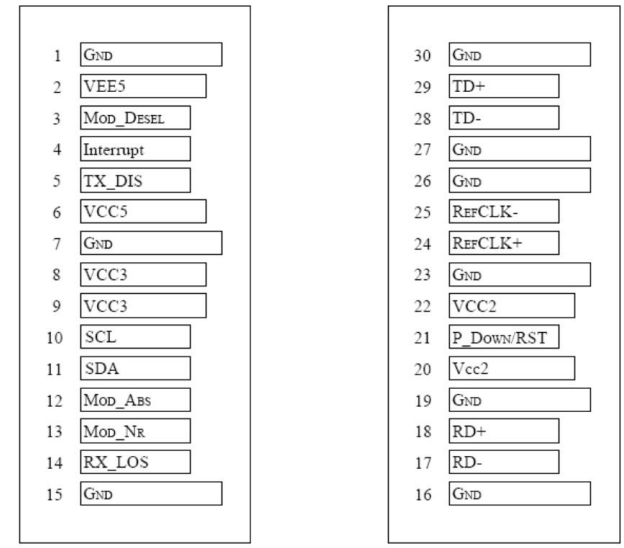
IV. Electrical Characteristics

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Supply Voltage	V_{CC}	3.13		3.45	V	
Supply Current	I_{CC}			500	mA	
Module Total Power	P			3.5	W	
Transmitter						
Input Differential Impedance	R_{IN}		100		Ω	1
Differential Data Input Swing	$V_{IN,pp}$	150		820	mV	
Transmit Disable Voltage	V_D	2		V_{CC}	V	
Transmit Enable Voltage	V_{EN}	G_{ND}		G_{ND}+0.8	V	
Transmit Disable Assert Time	T_off			100	ms	
Tx Enable Assert Time	T_on			100	ms	
Receiver						
Differential Data Output Swing	$V_{out,pp}$	300	500	850	mV	
Output Rise Time	t_{RISE}			35	ps	2
Output Fall Time	t_{FALL}			35	ps	2
LOS Fault	V_{LOSFT}	V_{CC} – 0.5		V_{CCHOST}	V	3
LOS Normal	V_{LOSNR}	G_{ND}		G_{ND}+0.5	V	3
Power Supply Rejection	PSR		See Note 4 below			4

Notes

1. After internal AC coupling.
2. 20 – 80 %
3. Loss of Signal is open collector to be pulled up with a 4.7k – 10kohm resistor to 3.15 – 3.6V. Logic 0 indicates normal operation; logic 1 indicates no signal detected.
4. Per Section 2.7.1. in the XFP MSA Specification.

V. Pin Description



Bottom of Board
(As view through top of board)

Top of Board

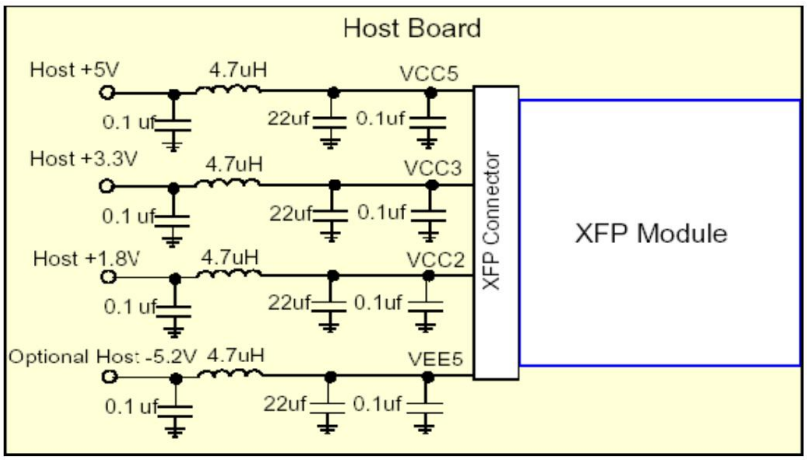
Pin Number	Logic	Symbol	Name/Description	Notes
1		G_{ND}	Module Ground	1
2		V_{EE5}	Optional –5.2 Power Supply – Not required	
3	LVTTL-I	Mod-Desel	Module De-select; When held low allows the module to respond to 2-wire serial interface commands	
4	LVTTL-O	Interrupt	Interrupt (bar); Indicates presence of an important condition which can be read over the serial 2-wire interface	2
5	LVTTL-I	TX_DIS	Transmitter Disable; Transmitter laser source turned off	
6		V_{CC5}	+5 Power Supply	
7		G_{ND}	Module Ground	1
8		V_{CC3}	+3.3V Power Supply	
9		V_{CC3}	+3.3V Power Supply	
10	LVTTL-I	SCL	Serial 2-wire interface clock	2
11	LVTTL-I/O	SDA	Serial 2-wire interface data line	2
12	LVTTL-O	Mod_Abs	Module Absent; Indicates module is not present. Grounded in the module	2
13	LVTTL-O	Mod_NR	Module Not Ready	2
14	LVTTL-O	RX_LOS	Receiver Loss of Signal indicator	2
15		G_{ND}	Module Ground	1

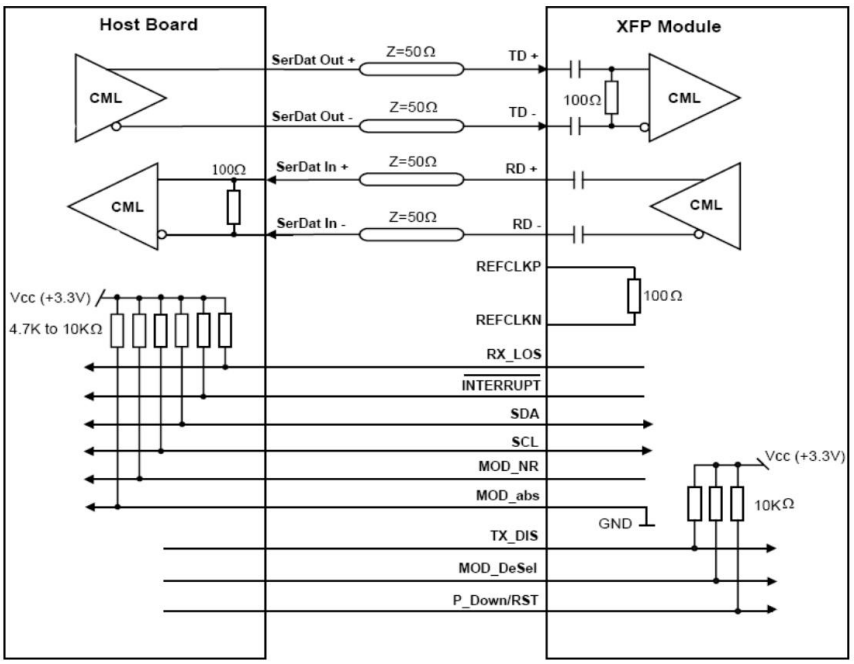
Pin Number	Logic	Symbol	Name/Description	Notes
16		G_{ND}	Module Ground	1
17	CML-O	RD-	Receiver inverted data output	
18	CML-O	RD+	Receiver non-inverted data output	
19		G_{ND}	Module Ground	1
20		V_{CC2}	+1.8V Power Supply – Not required	
21	LVTTL-I	P_Down/RST	Power Down; When high, places the module in the low power stand-by mode and on the falling edge of P_Down initiates a module reset Reset; The falling edge initiates a complete reset of the module including the 2-wire serial interface, equivalent to a power cycle	
22		V_{CC2}	+1.8V Power Supply – Not required	
23		G_{ND}	Module Ground	1
24	PECL-I	RefCLK+	Reference Clock non-inverted input, AC coupled on the host board – Not required	3
25	PECL-I	RefCLK-	Reference Clock inverted input, AC coupled on the host board –Not required	3
26		G_{ND}	Module Ground	1
27		G_{ND}	Module Ground	1
28	CML-I	TD-	Transmitter inverted data input	
29	CML-I	TD+	Transmitter non-inverted data input	
30		G_{ND}	Module Ground	1

Notes

1. Module circuit ground is isolated from module chassis ground within the module.
2. Open collector; should be pulled up with 4.7k – 10k ohms on host board to a voltage between 3.15Vand 3.45V.
3. A Reference Clock input is not required.

VI. Typical Application Circuit





VII. Diagram Mechanial Drawing