

# CFP2 100GBASE-LR4 1310nm 10km Transceiver Module

100G-CFP2-LR4-10KM-LL



## Application

- 100GE Routers and Switches
- 100G OTN
- 100G Network Security And Monitoring

## Features

- Hot Pluggable CFP2 MSA package
- IEEE 802.3ba 100GBASE-LR4 compliant
- CFP2 MSA Compliance
- ITU-T G.959.1 2012
- Up to 10km for G.652 SMF
- Cooled 4x25G LAN-WDM transmitter
- 4 x 28G Electrical Serial Interface (CEI-28G-VSR)
- MDIO management interface with Digital Diagnostic
- +3.3V power supply
- Power consumption less than 6W
- Compact size: 107.5x41.5x12.4 mm
- Operating case temperature: -5 to +70 °C
- Duplex LC Receptacle
- ROHS-6 compliant

## Description

Longline's CFP2-100G-LR4 transceivers are designed for use in 100 Gigabit Ethernet links over 10km single module fiber, and it compliant to the CFP MSA CFP2 HW Specification and IEEE 802.3ba 100GBASE-LR4. Digital diagnostics are available via MDIO as specified in the CFP MSA Management Interface Specification.

The transceiver's designs are optimized for high performance and cost efficiency to provide customers the best solutions for Datacom and Telecom applications.

The transceiver is RoHS-6 compliant and lead-free per Directive 2002/95/EC.

## Product Specifications

### I. Absolute Maximum Ratings

The limit of the maximum value is shown as below Table 1. (If operating out the limit of the maximum value will cause permanent damage).

Parameter	Symbol	Conditions	Min.	Max	Unit	Ref.
<b>Storage temperature(case)</b>	Tstg		-40	+85	°C	
<b>Relative humidity</b>	RH	0		85	%	
<b>Damage Threshold for Receiver</b>	Pmax			+10.0	dBm	
<b>Power Supply</b>	Vcc3.3V		-0.3	+3.6	V	
	Vcc5.0V				V	
<b>Input 3.3V LVCMOS signal level</b>	Vi		-0.3	Vcc+0.3	V	
<b>Input 1.2V LVCMOS signal level</b>	Vi		-0.3	1.6	V	
<b>ESD Sensitivity on module and all host pins</b>	HBM	Human Body model R=1.5K,C=100pF		2000	V	

## II. Recommended Operating Environment

The recommended working conditions are shown as below Table 2.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Ref.
<b>Operating Case Temperature</b>	T <sub>c</sub>	0		+70	°C	
<b>Supply voltage</b>	V <sub>cc 3.3V</sub>	+3.14	+3.3	+3.47	V	
<b>Power dissipation</b>	P			6	W	
<b>Low Power dissipation</b>	P <sub>Low</sub>			1	W	
<b>In-rush Curent</b>	I <sub>-inrush</sub>			200	mA/us	
<b>Turn-off rush Curent</b>	I <sub>-turnoff</sub>	-200			mA/us	
<b>Link Distance</b>	L	2M		10km	G.652 SMF	

## III. Optical Characteristics

Table 3 -100Gb/s CFP2 Optical Specifications (100GBase-LR4)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
<b>Transmitter</b>						
<b>Channel data rate</b>				25.7812		Gbps
<b>Aggregate data rate</b>				103.125		Gbps
<b>Data rate variation</b>			-100		+100	ppm
<b>Lane Center Wavelength</b>	λ <sub>cT0</sub>		1294.53	1295.56	1296.59	nm
	λ <sub>cT1</sub>		1299.02	1300.05	1301.09	nm
	λ <sub>cT2</sub>		1303.54	1304.58	1305.63	nm
	λ <sub>cT3</sub>		1308.09	1309.14	1310.19	nm
<b>Total Average Launch Power</b>	P <sub>out</sub>				10.5	dBm
<b>Average Launch Power per Lane</b>	P <sub>each</sub>		-4.3		4.5	dBm

<b>Optical Modulation Amplitude per Lane</b>	OMA		-1.3		4.5	dBm
<b>Difference in Launch power between any two lanes(OMA)</b>					5.0	dB
<b>Launch power in OMA minus TDP, per lane</b>	Poma tdp		-2.3			dBm
<b>Average Launch Power of TX_DIS Transmitter per lane</b>	Poff	TX_DIS=H			-30	dBm
<b>Extinction Ratio</b>	ER		4			dB
<b>SMSR</b>	SMSR		30			dB
<b>Dispersion Penalty</b>	DP	10km SMF			2.2	dB
<b>Relative Intensity Noise</b>	RIN	Mod off			-130	dB/Hz
<b>Optical Return Loss Tolerance</b>	TRL				20	dB
<b>Transmitter reflectance</b>	Tef				-12	dB
<b>Optical Eye Mask {X1, X2, X3, Y1, Y2, Y3}1</b>	EM		{0.25, 0.4, 0.45, 0.25, 0.28,0.4}			

### Receiver

<b>Channel data rate</b>				25.7812		Gbps
<b>Data rate variation</b>			-100		+100	ppm
<b>Lane Center Wavelength</b>	$\lambda_{cT0}$		1294.53	1295.56	1296.59	nm
	$\lambda_{cT1}$		1299.02	1300.05	1301.09	nm
	$\lambda_{cT2}$		1303.54	1304.58	1305.63	nm
	$\lambda_{cT3}$		1308.09	1309.14	1310.19	nm
<b>Damage threshold</b>	PDT			5.5		dBm
<b>Average receiver power per lane</b>	Rpow		-10.6		4.5	dBm
<b>Receive power OMA per Lane</b>	Rovl				4.5	dBm
<b>Difference in receive power between any two lanes(OMA)</b>					5.5	dB
<b>Receiver Sensitivity(OMA) per lane</b>	Psen				-8.6	dBm

**Stressed Receiver Sensitivity per Lane**

Psen\_str

-6.8

dBm

<b>Receiver Reflectance</b>	Ref				-26	dB
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**Conditions of stressed receiver sensitivity test**

<b>Vertical eye closure penalty per Lane</b>					1.8	dB
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**Stressed eye jitter per Lane**

0.3

UI

<b>Rx-Lane LOS Assert</b>			-25			dBm
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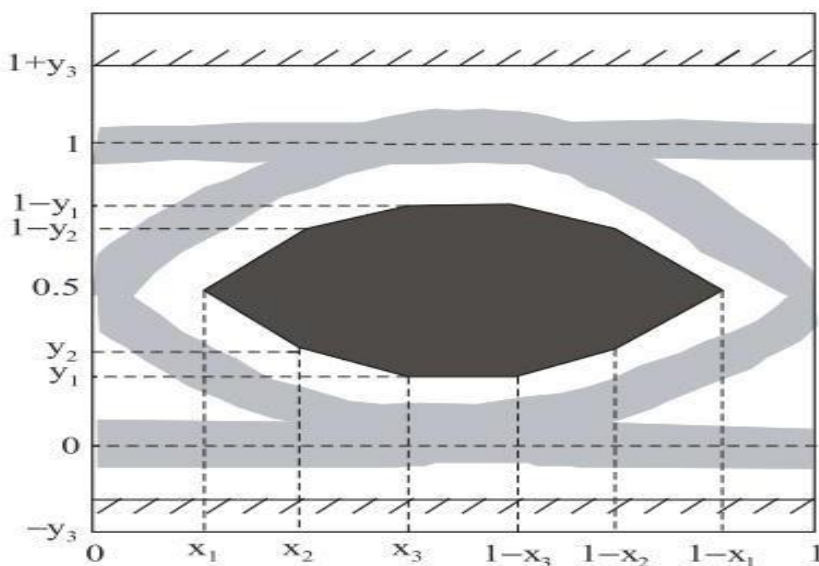
**Rx-Lane LOS De-assert**

-13

dBm

<b>Rx-Lane LOS Hysteresis</b>			0.5			dB
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**Note1.** Please refer to Figure 1



**Figure 1 - Transmission eye mask definition**

Table 4 - 100Gb/s CFP2 Optical Specifications (OTU4)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
<b>Transmitter</b>						
<b>Channel data rate</b>				27.9525		Gbps
<b>Aggregate data rate</b>				111.809		Gbps
<b>Data rate variation</b>			-20		+20	ppm
<b>Lane Center Wavelength</b>	$\lambda_{cT0}$		1294.53	1295.56	1296.59	nm
	$\lambda_{cT1}$		1299.02	1300.05	1301.09	nm
	$\lambda_{cT2}$		1303.54	1304.58	1305.63	nm
	$\lambda_{cT3}$		1308.09	1309.14	1310.19	nm
<b>Total Average Launch Power</b>	$P_{out}$				8.9	dBm
<b>Average Launch Power per Lane</b>	$P_{each}$		-2.5		2.9	dBm
<b>Optical Modulation Amplitude per Lane</b>	OMA		-1.2		4.5	dBm
<b>Difference in Launch power between any two lanes(OMA)</b>					5.0	dB
<b>Average Launch Power of TX_DIS Transmitter per lane</b>	$P_{off}$	TX_DIS=H			-30	dBm
<b>Extinction Ratio</b>	ER		7			dB
<b>SMSR</b>	SMSR		30			dB
<b>Relative Intensity Noise</b>	RIN	Mod off			-130	dB/Hz
<b>Optical Return Loss Tolerance</b>	TRL				20	dB
<b>Transmitter reflectance</b>	$T_{ef}$				-12	dB
<b>Optical Eye Mask {X1, X2, X3, Y1, Y2, Y3}</b> <sup>1</sup>	EM				{0.25, 0.4, 0.45, 0.25, 0.28, 0.4}	

## Receiver

<b>Channel data rate</b>				27.9525		Gbps
<b>Data rate variation</b>			-20		+20	ppm
<b>Lane Center Wavelength</b>	$\lambda_{cR0}$		1294.53	1295.56	1296.59	nm
	$\lambda_{cR1}$		1299.02	1300.05	1301.09	nm
	$\lambda_{cR2}$		1303.54	1304.58	1305.63	nm
	$\lambda_{cR3}$		1308.09	1309.14	1310.19	nm
<b>Damage threshold</b>	PDT			5.5		dBm
<b>Average receiver power per lane</b>	Rpow				4.5	dBm
<b>Receiver power OMA per lane</b>	Rovl				4.5	dBm
<b>Difference in receive power between any two lanes(OMA)</b>					5.5	dB
<b>Optical path penalty</b>					1.5	dB
<b>Receiver Sensitivity per lane<sup>2</sup></b>	Psen				-10.3	dBm
<b>Receiver Sensitivity(OMA) per lane<sup>2</sup></b>	Psen_OMA				-9.1	dBm
<b>Receiver Reflectance</b>	Ref				-26	dB
<b>Rx-Lane LOS Assert</b>			-25			dBm
<b>Rx-Lane LOS Deassert</b>					-13	dBm
<b>Rx-Lane LOS Hysteresis</b>			0.5			dB

**Note1.** Please refer to Figure 1

**Note2.** OTU-4 Rate, BER < 10-12 with FEC, ER > 7dB

## IV. Electrical Characteristics

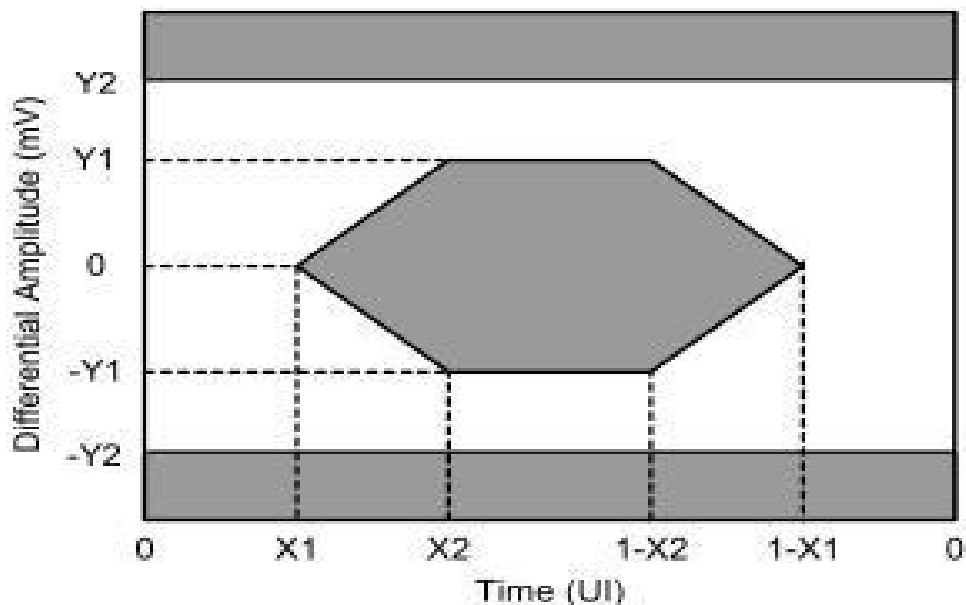
**Table 5 - 100Gb/s CFP2 Electrical High Speed I/O Interface Specifications**

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
<b>Transmitter (CAUI input interface)</b>						
Signal Rate Per Lane				25.78125		Gb/s
Signal Rate Tolerance			-100		100	ppm
AC Common Mode input Voltage Tolerance(RMS)					20	mV
Differential input returnloss	$RL_{diff}$	IEEE 802.3ba-2010		See Equation (83B-7)		dB
Total Input Jitter Tolerance	$T_{jin}$				0.62	UI
Deterministic Input Tolerance -Jitter	$T_{din}$				0.42	UI
Transmitter Input Mask (X1, X2)-Eye				(0.31, 0.5)		UI <sub>i</sub>
Transmitter Input Mask (Y1, Y2)-Eye				(42.5, 425)		mV <sub>i</sub>
<b>Receiver (CAUI output interface)</b>						
Signal Rate Per Lane				25.78125		Gb/s
Signal Rate Tolerance			-100		100	ppm
Single-ended output voltage	$V_{sig}$		-0.4		4	V
Output AC common-mode voltage(RMS)	$V_{comAC}$				15	mV
Output transition time	$T_r$	20%~80%	24			ps
Differential output returnloss		IEEE802.3ba-2010		See Equation (83B-5)		dB
Total Jitter	$T_j$				0.4	UI
Deterministic Jitter	$T_{dj}$				0.25	UI



<b>Receiver Output Eye Mask(X1, X2)</b>	(0.2,0.5)	UI <sup>2</sup>
<b>Receiver Output Eye Mask(Y1, Y2)</b>	(136,380)	mV <sup>2</sup>

**Note1.** refer to figure 2  
**Note2.** refer to figure 3



**Figure 3 - CAUI transmitter eye mask**

**Low Speed I/O interface**

**Table 6 -100Gb/s CFP2 3.3V LVCMOS Electrical Characteristics**

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
<b>Supply Voltage</b>	V <sub>CC</sub>		3.2	3.3	3.4	V
<b>Input High Voltage</b>	V <sub>IH</sub>		2		V <sub>CC</sub> +0.3	V
<b>Input Low Voltage</b>	V <sub>IL</sub>		-0.3		0.8	V
<b>Input Leakage Current</b>	I <sub>IN</sub>		-10		+10	mA
<b>Output High Voltage (IOH =-100uA)</b>	V <sub>OH</sub>		V <sub>CC</sub> -0.2		V <sub>CC</sub> +0.3	V

<b>Output Low Voltage (IOL =100uA)</b>	$V_{OL}$		-0.3		0.2	V
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<b>Minimum Pulse Width of Control Pin Signal</b>	$t_{CNTL}$		100			us
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Note:(MOD\_RSTn,MOD\_LOPWR,TX\_DIS,PRG\_CNTL,MOD\_ABS,RX\_LOS,GLB\_ALRMn, PRG\_ALRM ) are LVCMOS I/O interfaces.

**Table 7 - 100Gb/s CFP 1.2V LVCMOS Electrical Characteristics**

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
<b>Input High Voltage</b>	$V_{IH}$		0.84		1.5	V
<b>Input Low Voltage</b>	$V_{IL}$		-0.3		0.36	V
<b>Input Leakage Current</b>	$I_{IN}$		-100		+100	uA
<b>Output High Voltage</b>	$V_{OH}$		1.0		1.5	V
<b>Output Low Voltage</b>	$V_{OL}$		-0.3		0.2	V
<b>Output High Current</b>	$I_{OH}$				-4	mA
<b>Output Low Current</b>	$I_{OL}$		+4			mA
<b>Input capacitance</b>	$C_i$				10	pF

Note:(MDIO, MDC, PRTADR4:0) are 1.2V LVCMOS I/O interfaces

**Table 8 - 100Gb/s CFP Timing Parameters for CFP2 Hardware Signal Pins**

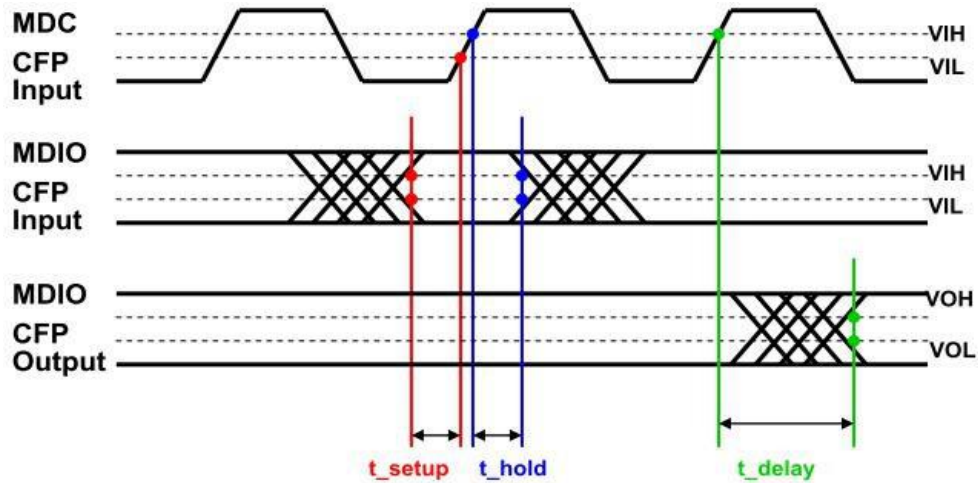
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
<b>HardwareMOD_LOPWR assert</b>	$t_{MOD\_LOPWR\_assert}$				1	ms
<b>Hardware MOD_LOPWR Deassert</b>	$t_{MOD\_LOPWR\_deassert}$				10	s
<b>Receiver Loss of Signal Assert Time</b>	$t_{loss\_assert}$				100	us

<b>Receiver Loss of Signal De-Assert Time</b>	t_loss_deassert				100	us
<b>Global Alarm Assert Delay Time</b>	GLB_ALRMn_assert				150	ms
<b>Global Alarm De-AssertDelay Time</b>	GLB_ALRMn_deassert				150	ms
<b>Management Interface ClockPeriod</b>	t_prd		250			ns
<b>Host MDIO t_setup</b>	t_setup		10			ns
<b>Host MDIO t_hold</b>	t_hold		10			ns
<b>CFP MDIO t_delay</b>	t_delay		0		175	ns
<b>Initialization time from Reset</b>	t_initialize				2.5	s
<b>Transmitter Disabled(TX_DIS asserted)</b>	t_de-assert				100	us
<b>Transmitter Enabled(TX_DIS de-asserted)</b>	t_assert				2	ms

**Table 9 - 100Gb/s CFP MDIO and MDC Timing Characteristics**

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
<b>Management Interface Clock Frequency</b>	F_MDC		0.1		4	MHz
<b>Management Interface Clock Period</b>	t_prd		250		10000	ns
<b>Host MDIO t_setup</b>	t_setup		10			ns
<b>Host MDIO t_hold</b>	t_hold		10			ns
<b>CFP MDIO t_delay1</b>	t_delay		0		175	ns
<b>MDC high and low time</b>	twidth		40		60	%
			160			ns
<b>MDIO/MDC termination in CFP</b>	Zt		100			kOhm

**Note1.** Delay from MDC rising edge to MDIO data change



**Figure 4 -100Gb/s CFP MDIO & MDC Timing Diagram**

**Clock interface**

**Table 10 - 100Gb/s CFP Reference Clock Characteristics**

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
<b>Impedance</b>	Zd		80	100	120	ohm
<b>Frequency</b>			1/64 of host lane rate			
<b>Frequency Stability</b>	Xf		-100		+100	ppm <sup>1</sup>
			-20		+20	ppm <sup>2</sup>
<b>Input Differential Voltage</b>	Vdiff		400		1200	mV <sup>3</sup>
<b>RMS Jitter</b>	$\sigma$				10	ps <sup>4</sup>
<b>Clock Duty Cycle</b>			40		60	%
<b>Clock Rise/Fall Time 10/90%</b>	Tr/f		200		1250	ps <sup>5</sup>

**Note1.** For Ethernet applications **Note2.** For Telecom applications

**Note3.** Peak to Peak Differential

**Note4.** Random Jitter. Over frequency band of 10kHz < f < 10MHz

**Note5.** 1/64 of electrical lane

**Table 11 - 100Gb/s CFP Transmitter & Receiver Monitor Clock Characteristics**

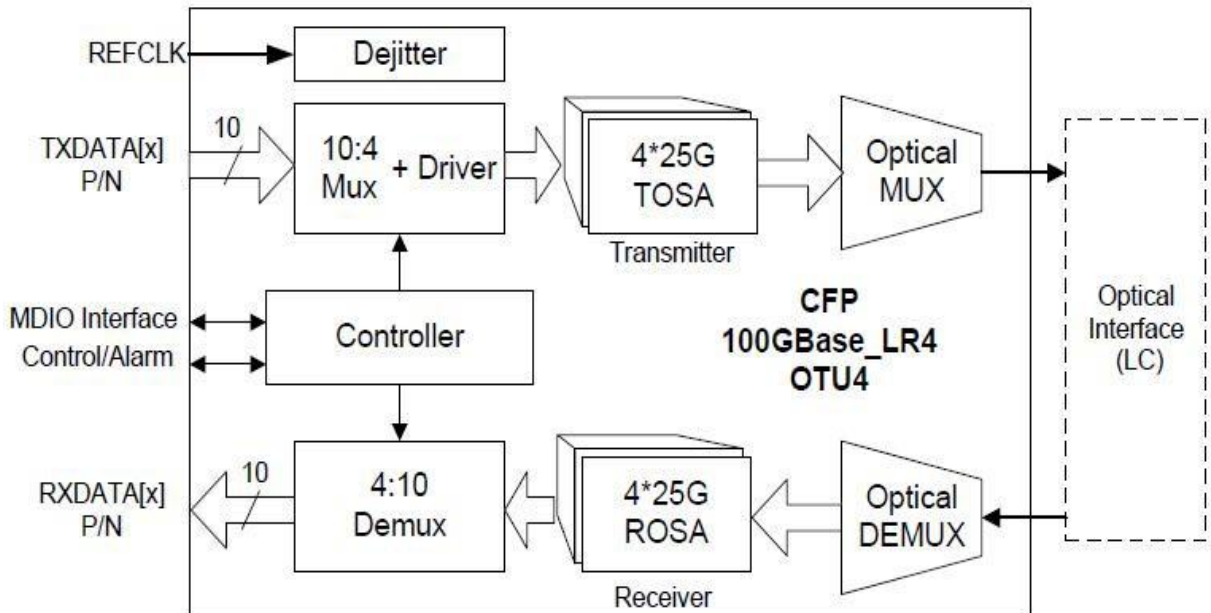
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
<b>Impedance</b>	Zd		80	100	120	ohm
<b>Frequency</b>			1/8 of network lane rate			
<b>Output Differential Voltage</b>	Vdiff		400		1200	mV <sup>1</sup>
<b>Clock Duty Cycle</b>			40		60	%

**Note1.** Peak to Peak Differential

## V. 100Gb/s CFP Function Diagram

### Internal reference structure

The internal structure of 100Gb/s CFP shown as Figure 5.



**Figure 5 -10km 100Gb/s CFP2 internal structure**

## VI.Recommended Interface Circuit

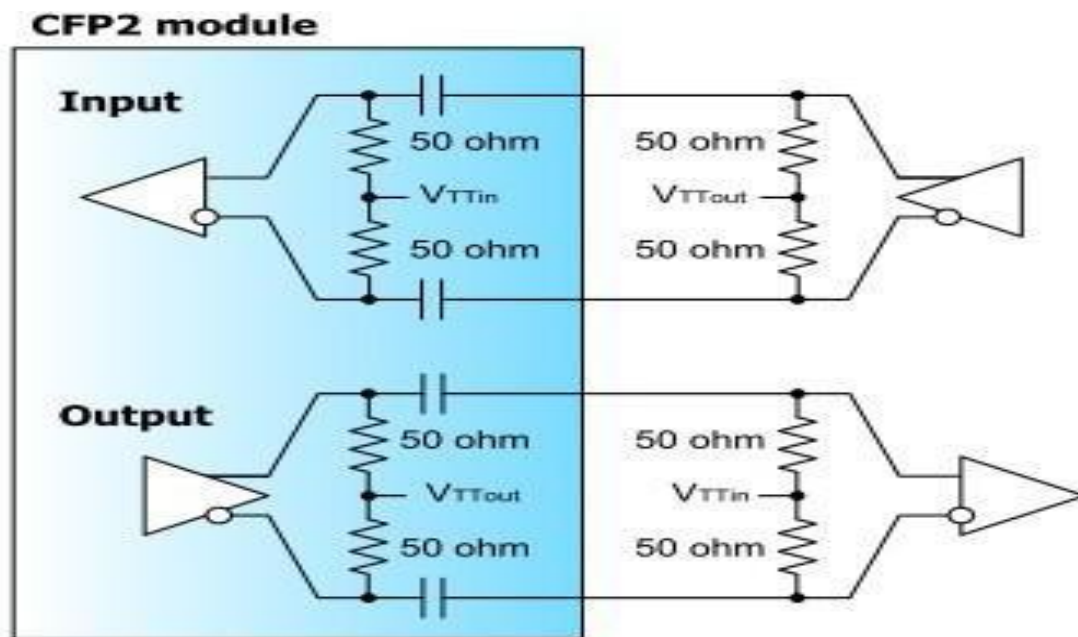


Figure 6 - Recommended High Speed I/O for Data and Clocks

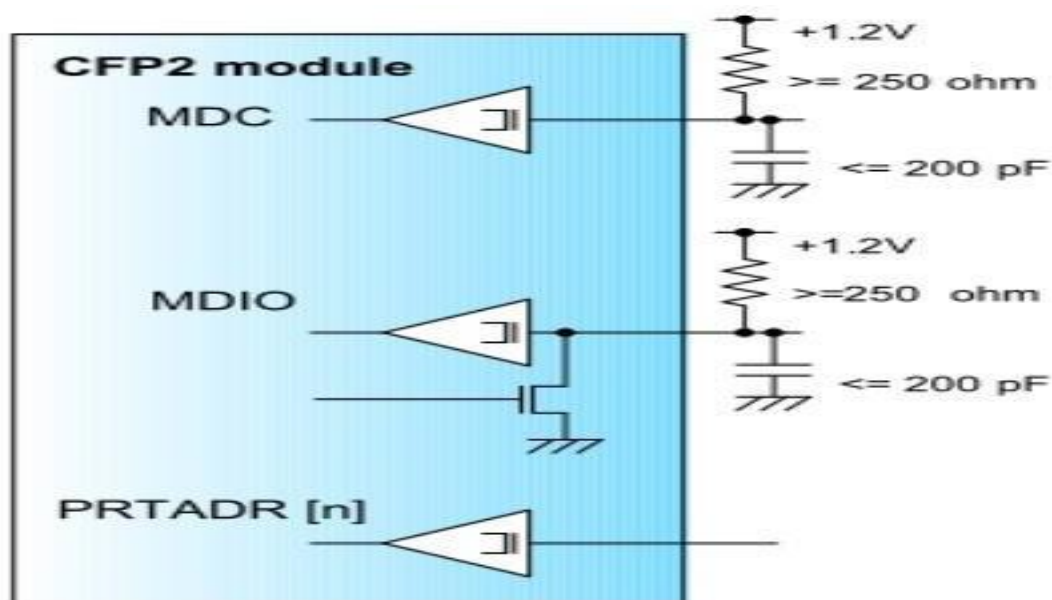
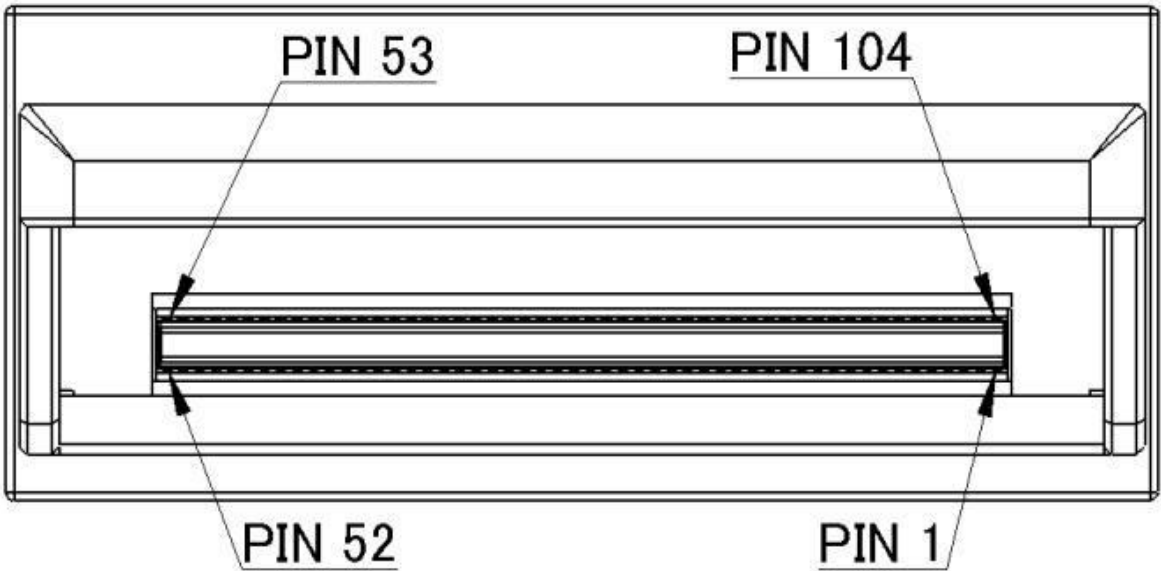
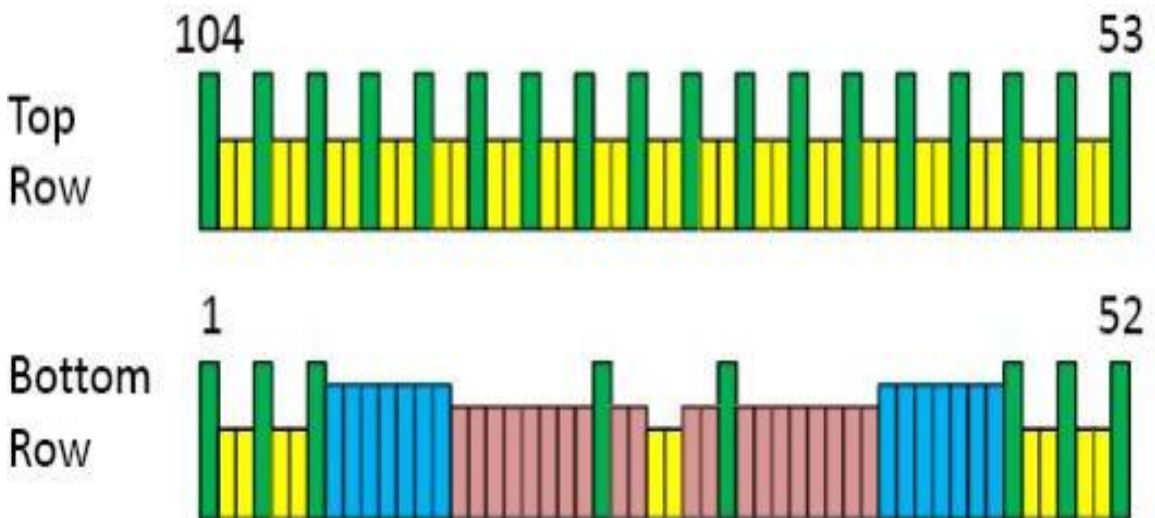


Figure 7 - Recommended MDIO Interface Termination

**VII.Pin Layout**



**Figure 8 - CFP2 Module Pad Layout**



### IX. 100Gb/s CFP Mechanical Specifications

100Gb/s CFP2 mechanical dimensions should be compliant with CFP2 MSA specification.

Detailed dimensions are shown in Figure 10.

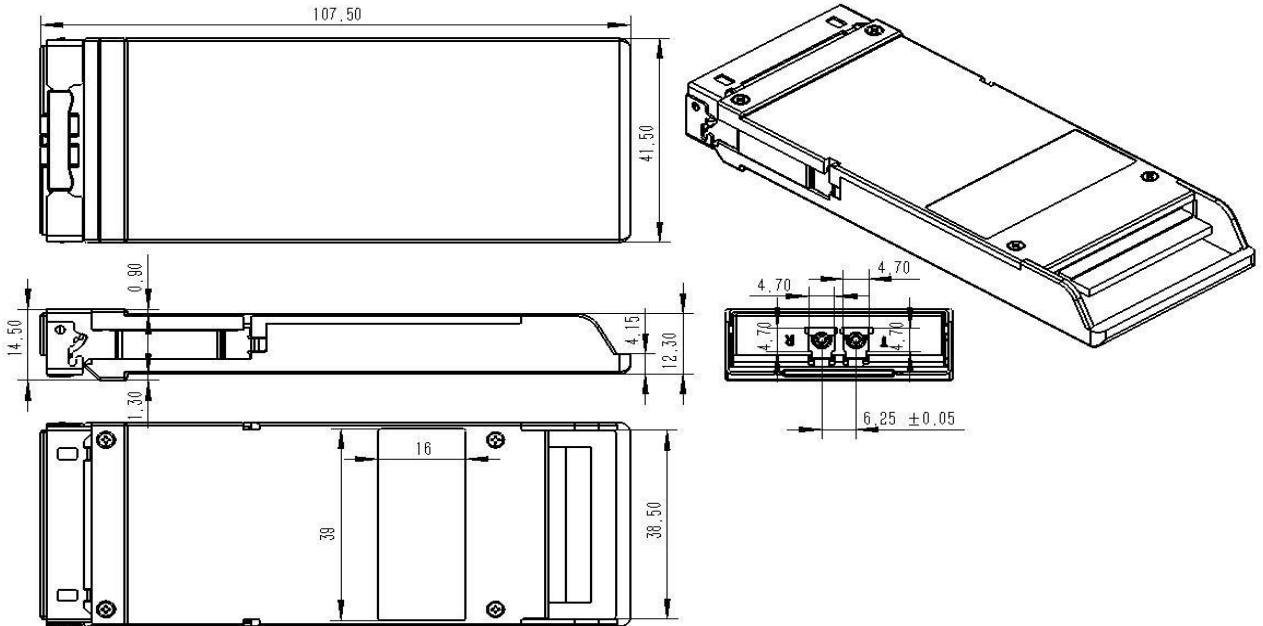


Figure 10 - 100Gb/s CFP2 Mechanical Dimensions(unit:mm)

### X. Management Interface

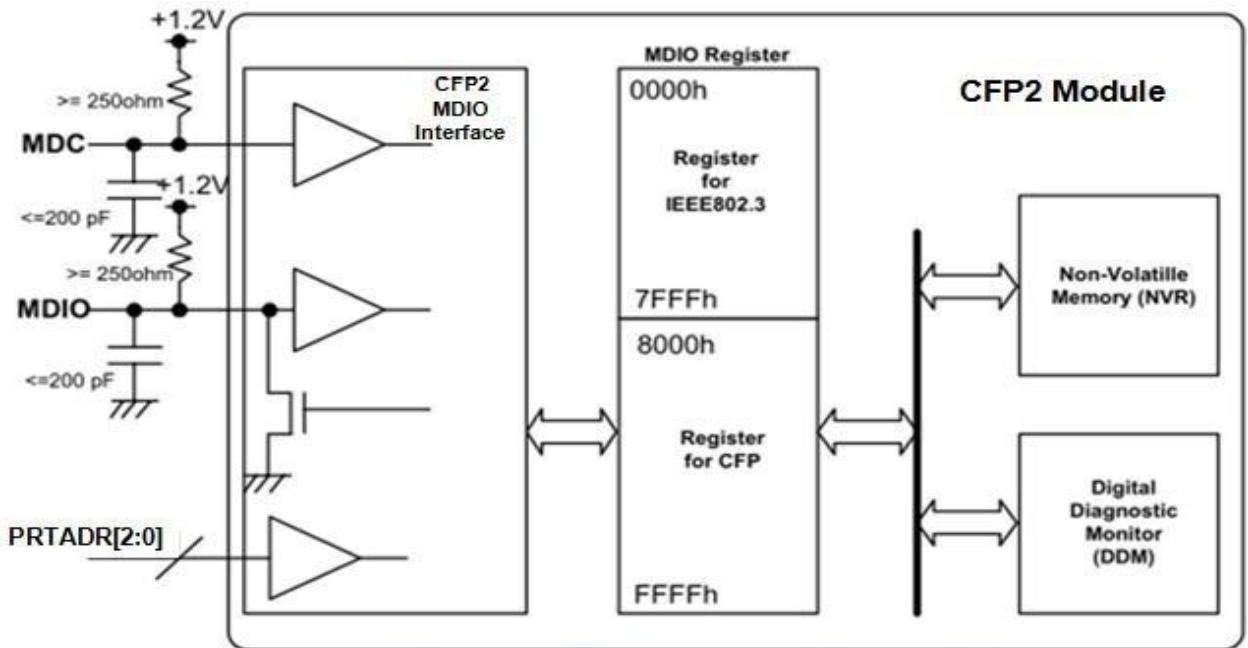


Figure 12 - CFP MDIO Interface