CFP 100GBASE-LR4 1310nm 10km Transceiver Module

100G-CFP-LR4-10-LL

Application

- 100GBase-LR4 Ethernet
- ITU-T OTU4

Features

- Hot Pluggable CFP MSA package
- IEEE 802.3ba 100GBASE-LR4 compliant
- CFP-MSA-HW-Spec-rev1-40 compliant
- Up to 10km for G.652 SMF
- Receiver: 4-lane×25Gb/s PIN ROSA
- Transmitter: 4-lane×25Gb/s LAN-WDM EML TOSA(1295.56,1300.05, 304.58,1309.14nm)
- 10x10G Electrical Serial Interface (CAUI/ OTL4.10)
- MDIO management interface with Digital Diagnostic
- +3.3V power supply
- Power consumption less than 12W
- Operating case temperature: 0 to +70 ℃
- Duplex SC or LC Receptacle
- ROHS-6 compliant

Description

Longline's CFP-LR4-100G transceivers are designed for use in 100 Gigabit Ethernet links over 10km single module fiber, and it compliant to the CFP MSA and IEEE 802.3ba 100GBASE-LR4. Digital diagnostics are available via MDIO as specified in the CFP MSA Management Interface Specification.

The transceiver's designs are optimized for high performance and cost efficiency to provide customers the best solutions for Datacom and Telecom applications.

The transceiver is RoHS-6 compliant and lead-free per Directive 2002/95/EC.

Transmitter Operation

The transceiver module receives 10 channels of 10Gb/s or 11.2Gb/s electrical data and converts them to 4 channels of 25Gb/s or 28Gb/s electrical data through a gearbox. The 4-channel electrical data are then processed by a 4-channel Clock and Data Recovery (CDR), which is integrated into the EML laser driver IC, for retiming and jitter reduction. Subsequently, the 4-channel EML laser driver drives the 4 cooled EML lasers, which are packaged in the Transmitter CFP-LR4-100G Sub-Assembly (TOSA), with the 4 channels of electrical signals. Each laser launches an CFP-LR4-100G signal in one of the four specific wavelengths as specified by IEEE802.3ba 100GBASE-LR4 requirements. These 4-lane CFP-LR4-100G signals will be CFP-LR4-100Gly multiplexed into a single fiber by a 4-to-1 CFP-LR4-100G WDM MUX. The CFP-LR4-100G output power of each channel is maintained constant by an automatic power control (APC) circuit. The transmitter output can be turned off by TX_DIS hardware signal and/or through MDIO module management interface.

Transmitter Operation

The receiver receives 4-lane LAN WDM CFP-LR4-100G signals. They are de-multiplexed by a 1-to-4 CFP-LR4-100G DEMUX and each of the resulting 4 channels of CFP-LR4-100G signals is fed into one of the 4 receivers that are packaged into the Receiver CFP-LR4-100G Sub-Assembly (ROSA). Each receiver converts the CFP-LR4-100G signal to an electrical signal. The regenerated electrical signals are retimed and de-jittered by a 4-channel CDR, which is integrated into the limiting amplifier IC, and amplified by the limiting amplifier. The 4 channels of 25Gb/s or 28Gb/s electrical data are then converted to 10 channels of 10Gb/s or 11.2Gb/s output electrical data by a gearbox. In addition, each received CFP-LR4-100G signal is monitored by the DOM section. The monitored value is reported through the MDIO section. If one or more received CFP-LR4-100G signal is weaker than the threshold level, RX_LOS hardware alarm will be triggered.

Product Specifications

I. Absolute Maximum Ratings

The limit of the maximum value is shown as below Table 1. (If operating out the limit of the maximum value will cause permanent damage).

Parameter	Symbol	Conditions	Min	Max	Unit
Storage Temperature(case)	Tstg		-40	+85	℃
Relative humidity	RH	0		85	%
Damage Threshold for Receiver	Pmax			+10.0	dBm
Power Supply	V_{cc} 3.3V		-0.3	+3.6	V
	V_{cc} 5.0V				V
Input 3.3V LVCMOS signal level	Vi		-0.3	V_{cc}+0.3	V
Input 1.2V LVCMOS signal level	Vi		-0.3	1.6	V
ESD Sensitivity on module and all host pins	HBM	Human Body model R=1.5K, C=100pF		2000	V

II. Recommended Operating Environment

The recommended working conditions are shown as below Table 2.

Parameter	Symbol	Min	Typ.	Max	Unit
Operating Case Temperature	T_c	0		+70	℃
Supply Voltage	V_{cc} 3.3V	+3.14	+3.3	+3.47	V
Supply Current	I_{cc} 3.3V			3.3	A
Power dissipation	P			12	W
Low Power dissipation	PLow			2	W
In-rush Curent	I-inrush			50	mA/us
Turn-off rush Curent	I-turnoff	-50			mA/us
Link Distance	L	2M		10km	G.652 SMF

III. CFP-LR4-100G Characteristics

Table 3 100Gb/s CFP-LR4-100G Specifications (100GBase-LR4)

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Transmitter						
Channel data rate				25.7812		Gbps
Aggregate data rate				103.125		Gbps
Data rate variation			-100		+100	ppm
Lane Center Wavelength	λcT0		1294.53	1295.56	1296.59	nm
	λcT1		1299.02	1300.05	1301.09	nm
	λcT2		1303.54	1304.58	1305.63	nm
	λcT3		1308.09	1309.14	1310.19	nm
Total Average Launch Power	Pout				10.5	dBm
Average Launch Power per Lane	Peach		-4.3		4.5	dBm
CFP-LR4-100G Modulation Amplitude per Lane	OMA		-1.3		4.5	dBm
Difference in Launch power between any two lances(OMA)					5.0	dB
Launch power in OMA minus TDP, per lane	Poma tdp		-2.3			dBm
Average Launch Power of TX_DIS Transmitter per lane	Poff	TX_DIS=H			-30	dBm
Extinction Ratio	ER		4	5.5		dB
SMSR	SMSR		30			dB
Dispersion Penalty	DP	10km SMF			2.2	dB
Relative Intensity Noise	RIN	Mod off			-130	dB/Hz
Opitcal Return Loss Tolerance	TRL				20	dB
Transmitter reflectance	Tef				-12	dB
CFP-LR4-100G Eye Mask {X1, X2, X3, Y1, Y2, Y3}1	EM		{0.25, 0.4, 0.45, 0.25, 0.28,0.4}			
Receiver						
Channel Data Rate				25.7812		Gbps

Data Rate Variation			-100		+100	ppm
Lane Center Wavelength	λcT0		1294.53	1295.56	1296.59	nm
	λcT1		1299.02	1300.05	1301.09	nm
	λcT2		1303.54	1304.58	1305.63	nm
	λcT3		1308.09	1309.14	1310.19	nm
Damage Threshold	PDT			5.5		dBm
Average Receiver Power per lane	Rpow		-10.6		4.5	dBm
Receive Power OMA per Lane	Rovl				4.5	dBm
Difference in receive power between any two lanes(OMA)					5.5	dB
Receiver Sensitivity(OMA) per lane	Psen				-8.6	dBm
Stressed Receiver Sensitivity per Lane	Psen_str				-6.8	dBm
Receiver Reflectance	Ref				-26	dB
Conditions of stressed receiver sensitivity test						
Vertical eye closure penalty per Lane					1.8	dB
Stressed eye jitter per Lane					0.3	UI
Rx-Lane LOS Assert				-18		dBm
Rx-Lane LOS De-assert				-15		dBm
Rx-Lane LOS Hysteresis			0.5			dB

Note1: Please refer to Figure 1

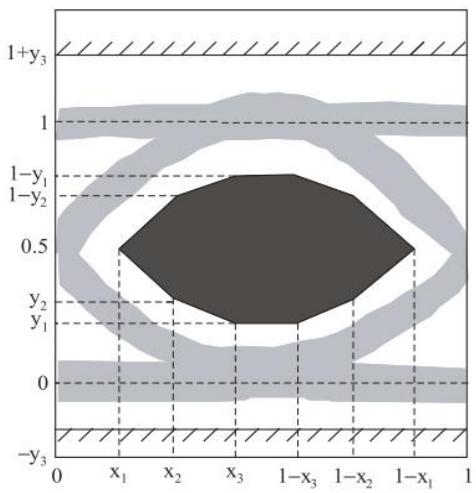

Figure 1-Transmission eye mask definition

Table 4 100Gb/s CFP CFP-LR4-100G Specifications (OTU4)

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Transmitter						
Channel data rate				27.9525		Gbps
Aggregate data rate				111.809		Gbps
Data rate variation			-20		+20	ppm
Lane Center Wavelength	λcT0		1294.53	1295.56	1296.59	nm
	λcT1		1299.02	1300.05	1301.09	nm
	λcT2		1303.54	1304.58	1305.63	nm
	λcT3		1308.09	1309.14	1310.19	nm
Total Average Launch Power	Pout				8.9	dBm
Average Launch Power per Lane	Peach		-2.5		2.9	dBm
CFP-LR4-100G Modulation Amplitude per Lane	OMA		-1.2		4.5	dBm
Difference in Launch power between any two lances(OMA)					5.0	dB
Average Launch Power of TX_DIS Transmitter per lane	Poff	TX_DIS=H			-30	dBm
Extinction Ratio	ER		7			dB
SMSR	SMSR		30			dB
Relative Intensity Noise	RIN	Mod off			-130	dB/Hz
Opitcal Return Loss Tolerance	TRL				20	dB
Transmitter reflectance	Tef				-12	dB
CFP-LR4-100G Eye Mask {X1, X2, X3, Y1, Y2, Y3}1	EM		{0.25, 0.4, 0.45, 0.25, 0.28,0.4}			
Receiver						
Channel Data Rate				27.9525		**Gbps**

Data Rate Variation			-20		+20	ppm
Lane Center Wavelength	λcR0		1294.53	1295.56	1296.59	nm
	λcR1		1299.02	1300.05	1301.09	nm
	λcR2		1303.54	1304.58	1305.63	nm
	λcR3		1308.09	1309.14	1310.19	nm
Damage Threshold	PDT			5.5		dBm
Average Receiver Power per lane	Rpow				4.5	dBm
Receive Power OMA per Lane	Rovl				4.5	dBm
Difference in receive power between any two lanes(OMA)					5.5	dB
CFP-LR4-100G path penalty					1,5	dB
Receiver Sensitivity per lane2	Psen				-10.3	dBm
Receiver Sensitivity(OMA) per lane2	Psen_OMA				-9.1	dBm
Receiver Reflectance	Ref				-26	dB
Rx-Lane LOS Assert				-18		dBm
Rx-Lane LOS Deassert				-15		dBm
Rx-Lane LOS Hysteresis			0.5			dB

IV. Electrical Characteristics

High Speed I/O interface

Table 5 100Gb/s CFP Electrical High Speed I/O Interface Specifications

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Transmitter (CAUI input interface)						
Signal Rate Per Lane				10.3125		Gb/s
Signal Rate Tolerance			-100		100	ppm
AC Common Mode input Voltage Tolerance(RMS)					20	mV
Differential input return loss	RI_{diff}	IEEE 802.3ba-2010	See Equation (83B–7)			dB
Total Input Jitter Tolerance	T_{jin}				0.62	UI
Deterministic Input Jitter Tolerance	T_{din}				0.42	UI
Transmitter Input Mask (X1, X2) Eye			(0.31, 0.5)			UI[1]
Transmitter Input Mask (Y1, Y2) Eye			(42.5, 425)			mV[1]
Receiver (CAUI output interface)						
Signal Rate Per Lane				10.3125		Gb/s
Signal Rate Tolerance			-100		100	ppm
Single-ended output voltage	Vosig		-0.4		4	V
Output AC common-mode voltage(RMS)	V_{ocomAC}				15	mV
Output transition time	Tr	20%~80%	24			ps
Differential output return loss		IEEE 802.3ba-2010	See Equation (83B–5)			dB
Total Jitter	T_j				0.4	UI
Deterministic Jitter	T_{dj}				0.25	UI
Receiver Output Eye Mask (X1, X2)				(0.2, 0.5)		UI[2]
Receiver Output Eye Mask (Y1, Y2)				(136, 380)		mV[2]

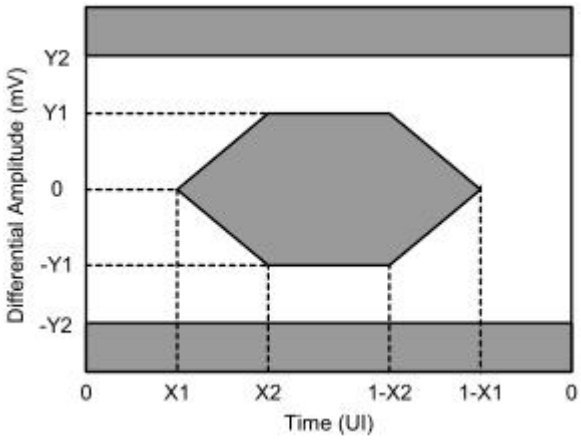

Figure 2-CAUI transmitter eye mask

Low Speed I/O interface

Table 6 100Gb/s CFP 3.3V LVCMOS Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Supply Voltage	V_{cc}		3.2	3.3	3.4	V
Input High Voltage	V_{IH}		2		V_{cc}+0.3	V
Input Low Voltage	V_{IL}		-0.3		0.8	V
Input Leakage Current	I_{IN}		-10		+10	mA
Output High Voltage (IOH =-100uA)	V_{OH}		V_{cc}-0.2		V_{cc}+0.3	V
Output Low Voltage (IOL =100uA)	V_{OL}		-0.3		0.2	V
Minimum Pulse Width of Control Pin Signal	t_CNTL		100			us

Notes: (MOD_RSTn,MOD_LOPWR,TX_DIS,PRG_CNTL,MOD_ABS,RX_LOS,GLB_ALRMn, PRG_ALRM) are LVCMOS I/O interfaces.

Table 7 100Gb/s CFP 1.2V LVCMOS Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Input High Voltage	V_{IH}		0.84		1.5	V
Input Low Voltage	V_{IL}		-0.3		0.36	V
Input Leakage Current	I_{IN}		-100		+100	uA
Output High Voltage	V_{OH}		1.0		1.5	V
Output Low Voltage	V_{OL}		-0.3		0.2	V
Output High Current	I_{OH}				-4	mA
Output Low Current	I_{OL}		+4			mA
Input capacitance	Ci				10	pF

Notes: (MDIO, MDC, PRTADR4:0) are 1.2V LVCMOS I/O interfaces

Table 8 100Gb/s CFP Timing Parameters for CFP Hardware Signal Pins

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Hardware MOD_LOPWR	t_MOD_LOPWR_assert				1	ms
Assert						
Hardware MOD LOPWR De-assert	t_MOD_LOPWR_deassert				10	s
Receiver Loss of Signal Assert Time	t_loss_assert				100	us
Receiver Loss of Signal De-Assert Time	t_loss_deassert				100	us
Global Alarm Assert Delay Time	GLB_ALRMn_assert				150	ms
Global AlarmDe-Assert Delay Time	GLB_ALRMn_deassert				150	ms
Management Interface Clock Period	t_prd		250			ns
Host MDIO t_setup	t_setup		10			ns
Host MDIO t_hold	t_hold		10			ns
CFP MDIO t_delay	t_delay		0		175	ns
Initialization time from Reset	t_initialize				2.5	s
Transmitter Disabled (TX_DIS asserted)	t_deassert				100	us
Transmitter Enabled (TX_DIS de-asserted)	t_assert				2	ms

Table 9 100Gb/s CFP MDIO and MDC Timing Characteristics

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Management Interface Clock Frequency	F_MDC		0.1		4	MHz
Management Interface Clock Period	t_prd		250		10000	ns
Host MDIO t_setup	t_setup		10			ns
Host MDIO t_hold	t_hold		10			ns
CFP MDIO t_delay1	t_delay		0		175	ns
MDC high and low time	twidth		40		60	%
			160			ns
MDIO/MDC termination in CFP	Zt		100			kOhm

Note1: Delay from MDC rising edge to MDIO data change

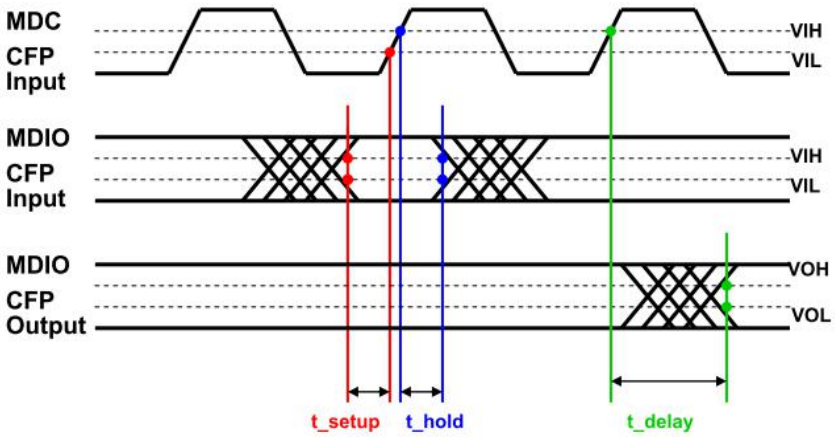

Figure 3-100Gb/s CFP MDIO & MDC Timing Diagram

Clock interface

Table 10 100Gb/s CFP Reference Clock Characteristics

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Impedance	Zd		80		100	120
Frequency				1/64 of host lane rate		
Frequency Stability	Xf		-100		+100	ppm[1]
			-20		+20	ppm[2]
Input Differential Voltage	Vdiff		400		1200	mV[3]
RMS Jitter	σ				10	ps[4]
Clock Duty Cycle			40		60	%
Clock Rise/Fall Time 10/90%	Tr/f		200		1250	ps[5]

Notes:

1.Delay from MDC rising edge to MDIO data change.

2.For Telecom applications.

3. Peak to Peak Differential.

4. Random Jitter. Over frequency band of 10kHz < f < 10MHz.

5. 1/64 of electrical lane.

Table 11 100Gb/s CFP Transmitter & Receiver Monitor Clock Characteristics

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Impedance	Zd		80	100	120	ohm
Frequency			1/8 of network lane rate			
Ouput Differential Voltage	Vdiff		400		1200	mV[1]
Clock Duty Cycle			40		60	%

V. 100Gb/s CFP Function Diagram

Internal reference structure

The internal structure of 100Gb/s CFP shown as Figure4.

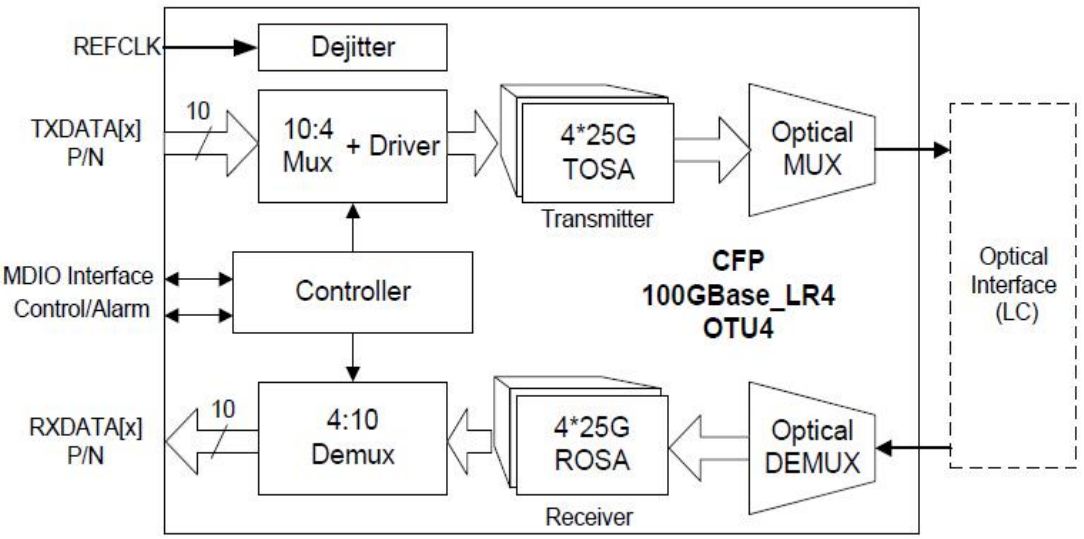

Figure 4-10km 100Gb/s CFP internal structure

Recommended Interface Circuit

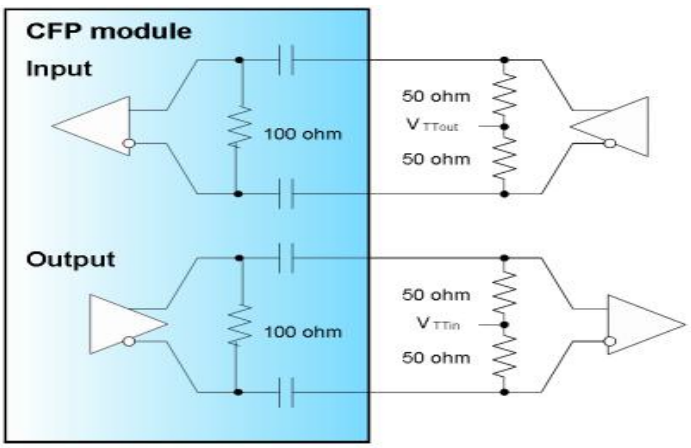

Figure 5-Recommended High Speed I/O for Data and Clocks

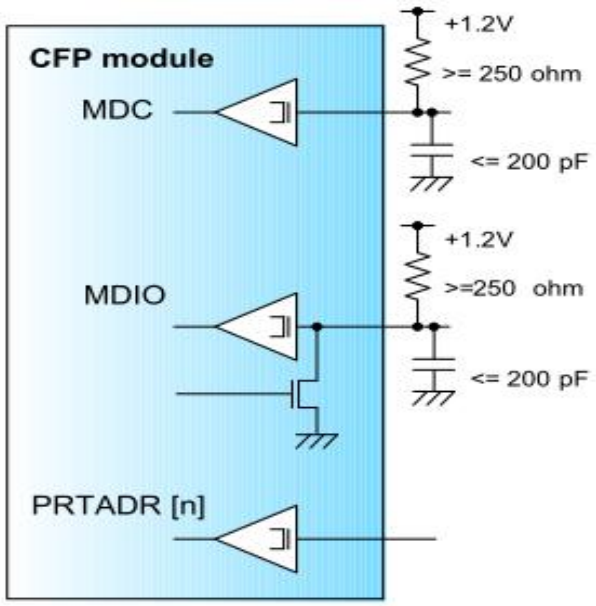

Figure 6-Recommended MDIO Interface Termination

Internal reference structure

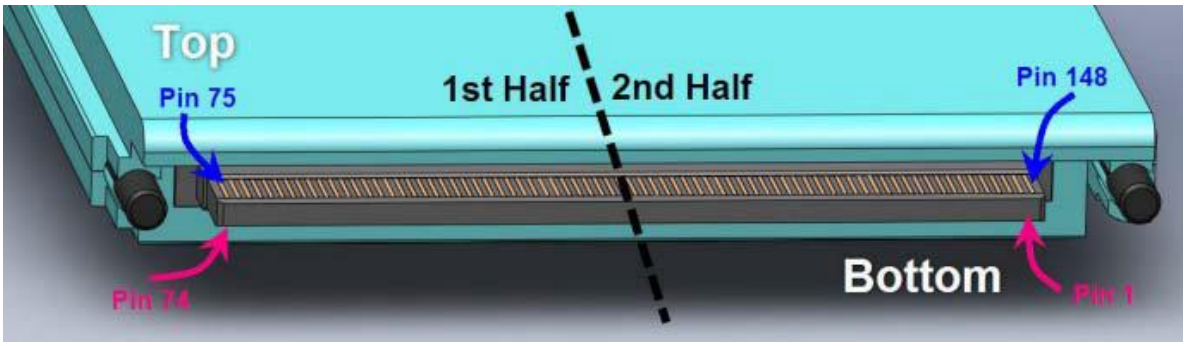

Figure 7-CFP Module Pad Layout

TOP ROW (2nd Half)			Bottom ROW (2nd Half)		TOP ROW (1st Half)		Bottom ROW (1st Half)
148	GND	1	3.3V_GND	111	GND	38	MOD_ABS
147	REFCLKn	2	3.3V_GND	110	N.C.	39	MOD_RSTn
146	REFCLKp	3	3.3V_GND	109	N.C.	40	RX_LOS
145	GND	4	3.3V_GND	108	GND	41	GLB_ALRMn
144	N.C.	5	3.3V_GND	107	RX9n	42	PRTADR4
143	N.C.	6	3.3V	106	RX9p	43	PRTADR3
142	GND	7	3.3V	105	GND	44	PRTADR2
141	TX9n	8	3.3V	104	RX8n	45	PRTADR1
140	TX9p	9	3.3V	103	RX8p	46	PRTADR0
139	GND	10	3.3V	102	GND	47	MDIO
138	TX8n	11	3.3V	101	RX7n	48	MDC
137	TX8p	12	3.3V	100	RX7p	49	GND
136	GND	13	3.3V	99	GND	50	VND_IO_F
135	TX7n	14	3.3V	98	RX6n	51	VND_IO_G
134	TX7p	15	3.3V	97	RX6p	52	GND
133	GND	16	3.3V_GND	96	GND	53	VND_IO_H
132	TX6n	17	3.3V_GND	95	RX5n	54	VND_IO_J
131	TX6p	18	3.3V_GND	94	RX5p	55	3.3V_GND
130	GND	19	3.3V_GND	93	GND	56	3.3V_GND
129	TX5n	20	3.3V_GND	92	RX4n	57	3.3V_GND
128	TX5p	21	VND_IO_A	91	RX4p	58	3.3V_GND
127	GND	22	VND_IO_B	90	GND	59	3.3V_GND
126	TX4n	23	GND	89	RX3n	60	3.3V
125	TX4p	24	(RX_MCLKn)	88	RX3p	61	3.3V
124	GND	25	(RX_MCLKp)	87	GND	62	3.3V
123	TX3n	26	GND	86	RX2n	63	3.3V
122	TX3p	27	VND_IO_C	85	RX2p	64	3.3V
121	GND	28	VND_IO_D	84	GND	65	3.3V
120	TX2n	29	VND_IO_E	83	RX1n	66	3.3V
119	TX2p	30	PRG_CNTL1	82	RX1p	67	3.3V

118	GND	31	PRG_CNTL2	81	GND	68	3.3V
117	TX1n	32	PRG_CNTL3	80	RX0n	69	3.3V
116	TX1p	33	PRG_ALRM1	79	RX0p	70	3.3V_GND
115	GND	34	PRG_ALRM2	78	GND	71	3.3V_GND
114	TX0n	35	PRG_ALRM3	77	(RX_MCLKn)	72	3.3V_GND
113	TX0p	36	TX_DIS	76	(RX_MCLKp)	73	3.3V_GND
112	GND	37	MOD_LOPWR	75	GND	74	3.3V_GND

Notes:

1.Pin 21,22,27,28,29,50,51,53,54 are internally used and NOT allowed to connect any signal and power supply or GND

2: Pin 24,25,76,77 are disabled unless MCLK output is enabled via MDIO

Pin Definition

Table 12 100Gb/s CFP Pin Definition(Bottom raw)

PIN	Name	I/O	Logic	Description
1	3.3V_GND			
2	3.3V_GND			
3	3.3V_GND			3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal Ground
4	3.3V_GND			
5	3.3V_GND			
6	3.3V			3.3V Module Supply Voltage
7	3.3V			3.3V Module Supply Voltage
8	3.3V			3.3V Module Supply Voltage
9	3.3V			3.3V Module Supply Voltage
10	3.3V			3.3V Module Supply Voltage
11	3.3V			3.3V Module Supply Voltage
12	3.3V			3.3V Module Supply Voltage
13	3.3V			3.3V Module Supply Voltage
14	3.3V			3.3V Module Supply Voltage
15	3.3V			3.3V Module Supply Voltage

16	3.3V_GND			3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal Ground
17	3.3V_GND			
18	3.3V_GND			
19	3.3V_GND			
20	3.3V_GND			
21	VND_IO_A	I/O		Module Vendor I/O. Must No Connect at host board
22	VND_IO_B	I/O		Module Vendor I/O. Must No Connect at host board
23	GND			
24	TX_MCLKn	O	CML	TX Monitor Clock Output (Negative)
25	TX_MCLKp	O	CML	TX Monitor Clock Output (Positive)
26	GND			
27	VND_IO_C	I/O		Module Vendor I/O. Must No Connect at host board
28	VND_IO_D	I/O		Module Vendor I/O. Must No Connect at host board
29	VND_IO_E	I/O		Module Vendor I/O. Must No Connect at host board
30	PRG_CNTL1	I	LV CMOSw/ PUR	Programmable Control 1 set over MDIO, MSA Default: TRXIC_RSTn, TX & RX ICs reset, "0": reset, "1" or NC: enabled = not used 4.75kohm pull up in the module
31	PRG_CNTL2	I	LV CMOSw/ PUR	Programmable Control 2 set over MDIO, MSA Default: Hardware Interlock LSB, "00": ≤8W, "01":≤16W, "10": ≤24W, "11" or NC: ≤32W = not used 4.75kohm pull up in the module
32	PRG_CNTL3	I	LV CMOSw/ PUR	Programmable Control 3 set over MDIO, MSA Default: Hardware Interlock MSB, "00": ≤8W, "01": ≤16W, "10": ≤24W, "11" or NC: ≤32W = not used4.75kohm pull up in the module
33	PRG_ALRM1	O	LV CMOS	Programmable Alarm 1 set over MDIO, MSA Default: HIPWR_ON, "1": module power up completed, "0": module not high powered up
34	PRG_ALRM2	O	LV CMOS	Programmable Alarm 2 set over MDIO, MSA Default: MOD_READY, "1": Ready, "0": not Ready.
35	PRG_ALRM3	O	LV CMOS	Programmable Alarm 3 set over MDIO, MSA Default: MOD_FAULT, fault detected, "1": Fault, "0": No Fault
36	TX_DIS	I	LV CMOSw/ PUR	Transmitter Disable for all lanes, "1" or NC = transmitter disabled, "0" = transmitter enabled
37	MOD_LOPWR	I	LV CMOSw/ PUR	Module Low Power Mode. "1" or NC: module in low power (safe) mode, "0": power-on enabled 4.75kohm pull up in the module
38	MOD_ABS	O	GND	Module Absent."1" or NC: module absent, "0":module present, Pull Up Resistor on Host
39	MOD_RSTn	I	LV CMOSw/ PDR	Module Reset. "0" resets the module, "1" or NC = module enabled, 4.75kohm Pull Down Resistor in Module
40	RX_LOS	O	LV CMOS	Receiver Loss of CFP-LR4-100G Signal, "1": low CFP-LR4-100G signal, "0": normal condition
41	GLB_ALRMn	O	LV CMOS	Global Alarm. "0": alarm condition in any MDIO Alarm register, "1": no alarm condition, Open Drain, Pull Up Resistor on Host
42	PRTADR4	I	1.2V CMOS	MDIO Physical Port address bit 4

43	PRTADR3	I	1.2V CMOS	MDIO Physical Port address bit 3
44	PRTADR2	I	1.2V CMOS	MDIO Physical Port address bit 2
45	PRTADR1	I	1.2V CMOS	MDIO Physical Port address bit 1
46	PRTADR0	I	1.2V CMOS	MDIO Physical Port address bit 0
47	MDIO	I/O	1.2V CMOS	Management Data I/O bi-directional data (electrical specs as per 802.3ae and ba)
48	MDC	I	1.2V CMOS	Management Data Clock (electrical specs as per 802.3ae and ba)
49	GND			
50	VND_IO_F	I/O		Module Vendor I/O. Must No Connect at host board
51	VND_IO_G	I/O		Module Vendor I/O. Must No Connect at host board
52	GND			
53	VND_IO_H	I/O		Module Vendor I/O. Must No Connect at host board
54	VND_IO_J	I/O		Module Vendor I/O. Must No Connect at host board
55	3.3V_GND			3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal Ground
56	3.3V_GND			
57	3.3V_GND			
58	3.3V_GND			
59	3.3V_GND			
60	3.3V			3.3V Module Supply Voltage
61	3.3V			3.3V Module Supply Voltage
62	3.3V			3.3V Module Supply Voltage
63	3.3V			3.3V Module Supply Voltage
64	3.3V			3.3V Module Supply Voltage
65	3.3V			3.3V Module Supply Voltage
66	3.3V			3.3V Module Supply Voltage
67	3.3V			3.3V Module Supply Voltage
68	3.3V			3.3V Module Supply Voltage
69	3.3V			3.3V Module Supply Voltage
70	3.3V_GND			3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal Ground
71	3.3V_GND			
72	3.3V_GND			
73	3.3V_GND			
74	3.3V_GND			

Table 13 100Gb/s CFP Pin Definition(Top raw)

PIN	Name	I/O	Logic	Description
75	GND			
76	RX_MCLKp	O		RX Monitor Clock Output (Positive)
77	RX_MCLKn	O		RX Monitor Clock Output (Negative)
78	GND			
79	RX0p	O	HS I/O	Lane 0 Receiver Output (Positive)
80	RX0n	O	HS I/O	Lane 0 Receiver Output (Negative)
81	GND			
82	RX1p	O	HS I/O	Lane 1 Receiver Output (Positive)
83	RX1n	O	HS I/O	Lane 1 Receiver Output (Negative)
84	GND			
85	RX2p	O	HS I/O	Lane 2 Receiver Output (Positive)
86	RX2n	O	HS I/O	Lane 2 Receiver Output (Negative)
87	GND			
88	RX3p	O	HS I/O	Lane 3 Receiver Output (Positive)
89	RX3n	O	HS I/O	Lane 3 Receiver Output (Negative)
90	GND			
91	RX4p	O	HS I/O	Lane 4 Receiver Output (Positive)
92	RX4n	O	HS I/O	Lane 4 Receiver Output (Negative)
93	GND			
94	RX5p	O	HS I/O	Lane 5 Receiver Output (Positive)
95	RX5n	O	HS I/O	Lane 5 Receiver Output (Negative)
96	GND			
97	RX6p	O	HS I/O	Lane 6 Receiver Output (Positive)
98	RX6n	O	HS I/O	Lane 6 Receiver Output (Negative)
99	GND			
100	RX7p	O	HS I/O	Lane 7 Receiver Output (Positive)
101	RX7n	O	HS I/O	Lane 7 Receiver Output (Negative)
102	GND			
103	RX8p	O	HS I/O	Lane 8 Receiver Output (Positive)
104	RX8n	O	HS I/O	Lane 8 Receiver Output (Negative)
105	GND			
106	RX9p	O	HS I/O	Lane 9 Receiver Output (Positive)
107	RX9n	O	HS I/O	Lane 9 Receiver Output (Negative)

108	GND			
109	NC			Not Connected Internally
110	NC			Not Connected Internally
111	GND			
112	GND			
113	TX0p	I	HS I/O	Lane 0 Transmitter Input (Positive)
114	TX0n	I	HS I/O	Lane 0 Transmitter Input (Negative)
115	GND			
116	TX1p	I	HS I/O	Lane 1 Transmitter Input (Positive)
117	TX1n	I	HS I/O	Lane 1 Transmitter Input (Negative)
118	GND			
119	TX2p	I	HS I/O	Lane 2 Transmitter Input (Positive)
120	TX2n	I	HS I/O	Lane 2 Transmitter Input (Negative)
121	GND			
122	TX3p	I	HS I/O	Lane 3 Transmitter Input (Positive)
123	TX3n	I	HS I/O	Lane 3 Transmitter Input (Negative)
124	GND			
125	TX4p	I	HS I/O	Lane 4 Transmitter Input (Positive)
126	TX4n	I	HS I/O	Lane 4 Transmitter Input (Negative)
127	GND			
128	TX5p	I	HS I/O	Lane 5 Transmitter Input (Positive)
129	TX5n	I	HS I/O	Lane 5 Transmitter Input (Negative)
130	GND			
131	TX6p	I	HS I/O	Lane 6 Transmitter Input (Positive)
132	TX6n	I	HS I/O	Lane 6 Transmitter Input (Negative)
133	GND			
134	TX7p	I	HS I/O	Lane 7 Transmitter Input (Positive)
135	TX7n	I	HS I/O	Lane 7 Transmitter Input (Negative)
136	GND			
137	TX8p	I	HS I/O	Lane 8 Transmitter Input (Positive)
138	TX8n	I	HS I/O	Lane 8 Transmitter Input (Negative)
139	GND			
140	TX9p	I	HS I/O	Lane 9 Transmitter Input (Positive)
141	TX9n	I	HS I/O	Lane 9 Transmitter Input (Negative)
142	GND			

143	NC			Not Connected Internally
144	NC			Not Connected Internally
145	GND			
146	REFCLKp	I		Reference Clock Input (Positive)
147	REFCLKn	I		Reference Clock Input (Negative)
148	GND			

VI.100Gb/s CFP Mechanical Specifications

100Gb/s CFP mechanical dimensions should be compliant with CFP MSA specification.
Detailed dimensions are shown in Figure 8.

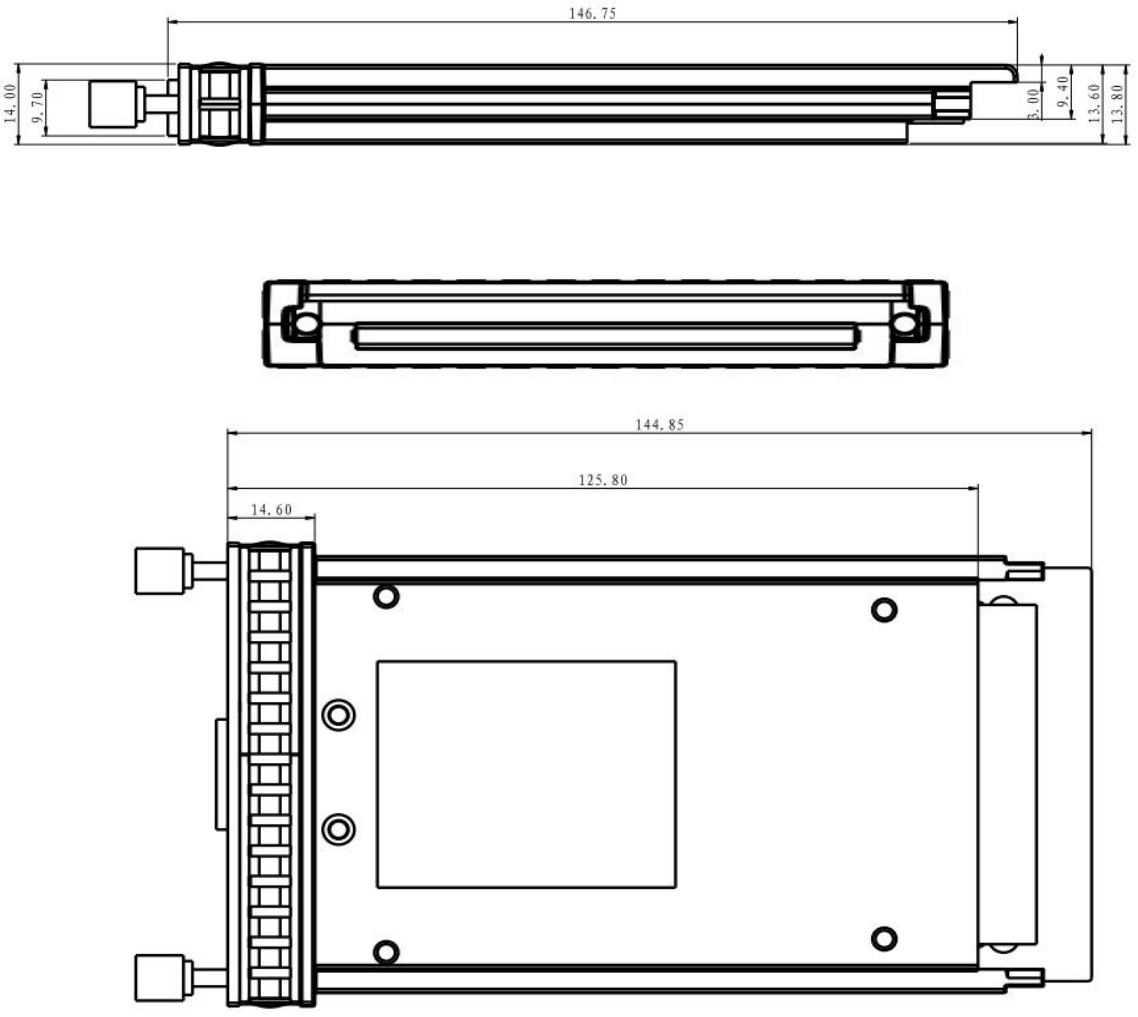

Figure 8-100Gb/s CFP Mechanical Dimensions(unit:mm)